

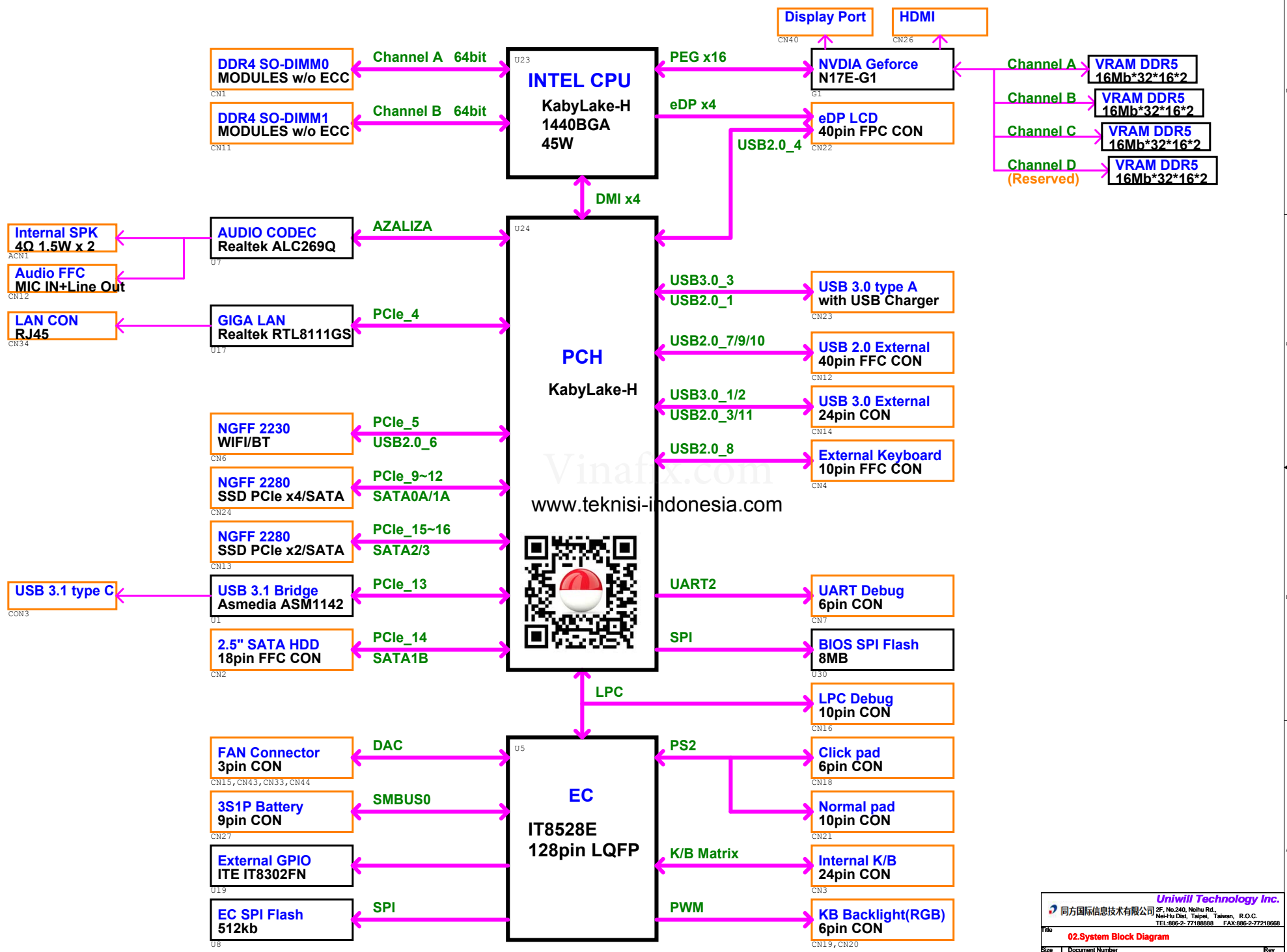
Platform : KBL_H+N17E

M/B Schematic Version Change List

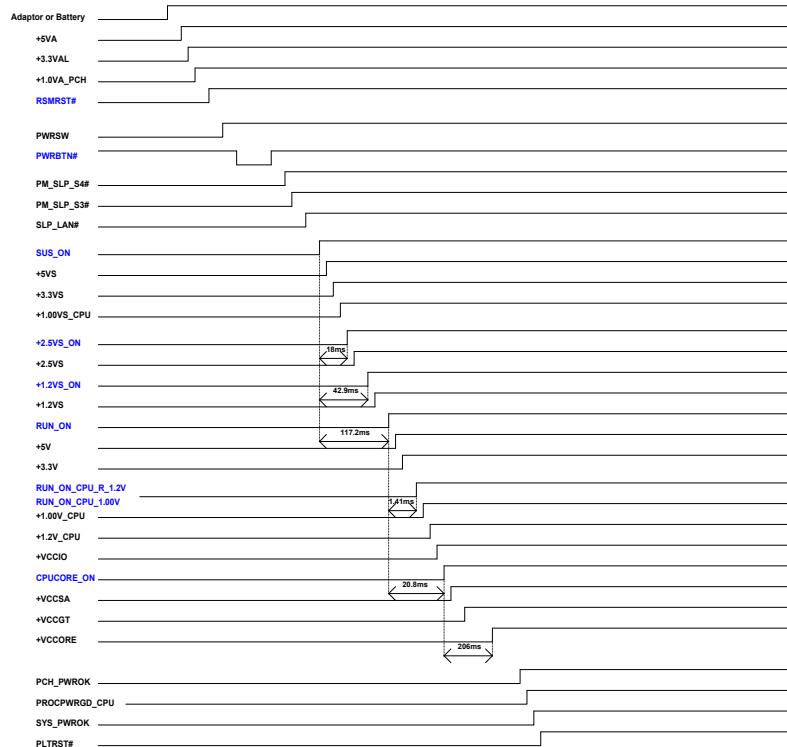
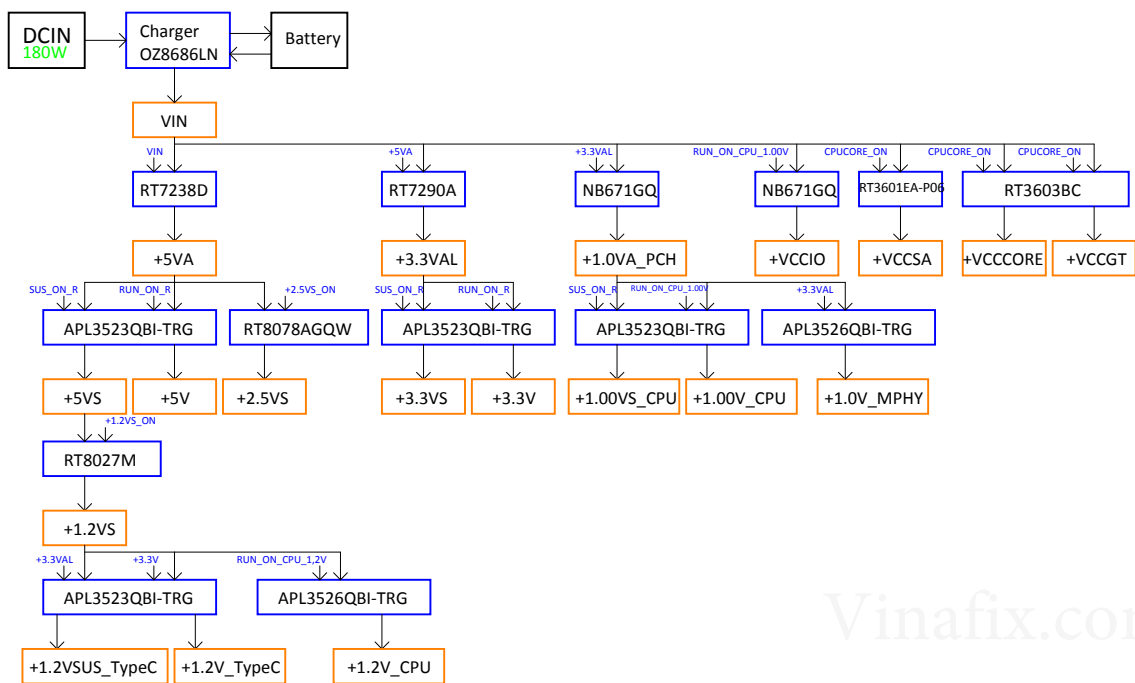
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| 33 | LAN PHY(RTL8118AG) | | |
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| 35 | EXT_MIC/USB/FAN/G-sen | | |
| 36 | BATT IN/CHARGER(OZ8686) | | |
| 37 | DC IN/D-Resis/HOLE/Debug | | |
| 38 | +5VA/+3.3VAL | | |
| 39 | +1.0VA_PCH/VCCIO | | |
| 40 | VCC SW | | |

[illegible]

SYSTEM BLOCK DIAGRAM



POWER BLOCK DIAGRAM



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EC IT8528E_FX

| Function1 | Function2 | Function3 | GPIO | Pin | Function | Net Name | Internal PU/PD | External PU/PD | Active |
|-----------|-----------|---------------|------|-----|----------------|-----------------|----------------|---|--------|
| PWM0 | WU43 | | GPIO | 24 | PWM | PWM_KB_LED_G | | | |
| PWM1 | WU44 | | GPIO | 25 | PWM | TP_LED_PWM | | | |
| PWM2 | WU45 | | GPIO | 26 | PWM | PWM_KB_LED_B | | | |
| PWM3 | WU32 | | GPIO | 29 | PWM | PWM_KB_LED_R | | | |
| PWM4 | WU33 | | GPIO | 30 | PWM | PD_1_CHG_R_LED | | | |
| PWM5 | WU34 | | GPIO | 31 | PWM | PD_2_PWM_LED | | | |
| PWM6 | WU35 | SSCK | GPIO | 32 | PWM | ME_KB_LED | | | |
| PWM7 | WU52 | RSG1# | GPIO | 34 | x | | | | |
| RXD | WU53 | SRD | GPIO | 108 | GPI | PM_SLP_S4# | | | Low |
| TXD | WU54 | SOUT0 | GPIO | 109 | GPI | PM_SLP_S3# | | | Low |
| CTD | WU36 | TMA0 | GPIO | 123 | GPO | GPO_Adaptor_In | | Pull-up 100K to +3.3V | |
| SMCLK | WU55 | | GPIO | 110 | GPO | BAT_SMBCLK | | Pull-up 4.7K to +3.3V | |
| SMDAT0 | WU46 | | GPIO | 111 | GPO | BAT_SMDAT | | Pull-up 4.7K to +3.3V | |
| GA20 | WU56 | | GPIO | 126 | H_A20GATE | | | Pull-up 10K to +3.3V | |
| RG1# | WU57 | | GPIO | 4 | H_RG1# | | | Pull-up 10K to +3.3V | Low |
| RG2# | WU58 | | GPIO | 112 | SAFETY_PROTECT | | | Pull-down 10K to GND | High |
| CRD0 | WU37 | | GPIO | 119 | GPO | LAN_PWR | | | High |
| SMCLK1 | WU59 | | GPIO | 115 | GPO | SMCLK_EC | | Pull-up 4.02K to +3.3V | |
| SMDAT1 | WU47 | | GPIO | 116 | GPO | SMDAT_EC | | Pull-up 4.02K to +3.3V | |
| KSO18 | WU60 | SMOS | GPIO | 56 | GPO | SENBIAT_V | | Pull-down 220K to GND | High |
| TMR0 | WU62 | | GPIO | 120 | GPO | FAN_enable0 | | | High |
| KSO17 | WU61 | SM50 | GPIO | 57 | GPO | SYS_PWRON | | | High |
| TMR1 | WU63 | | GPIO | 124 | GPO | PANEL_3.3V_ON | | Pull-down 100K to GND | High |
| PWUREG# | WU68 | BBO/SMCLK2ALT | GPIO | 18 | GPO | +2.5V_ON | | | High |
| RT1# | WU30 | | GPIO | 18 | GPI | ADAP_IN | | | High |
| RSG | WU41 | | GPIO | 24 | GPO | PWRST# | | | Low |
| UPCRST# | WU4 | | GPIO | 22 | GPI | P.LT_RST# | | | Low |
| ECSC# | WU62 | | GPIO | 23 | GPI | HDMI_HPD | | | Low |
| ECSS# | WU63 | | GPIO | 15 | ECSS# | EC_EXTSM# | | Pull-up 10K to +3.3V | Low |
| DR1 | WU64 | CTD0# | GPIO | 13 | GPIO | ME_VEN | | | Low |
| TACH0A | WU65 | | GPIO | 47 | TACH0A | FAN_SPD_DETECT0 | | | |
| TACH1A | WU69 | TMA1 | GPIO | 48 | TACH1A | FAN_SPD_DETECT1 | | | |
| LB0HLAT | WU24 | BA0 | GPIO | 19 | GPI | LDI# | | | Low |
| EGAD | WU25 | | GPIO | 82 | EGAD | ISAD | | | |
| EGCS# | WU26 | | GPIO | 83 | EGCS# | ISAS | | | Low |
| EGCLK | WU27 | | GPIO | 84 | EGCLK | ISCLK | | | |
| PWRSW | WU66 | | GPIO | 125 | PWRSW | PWRSW | | Pull-up 47K to +3.3V | Low |
| UPCPD# | WU6 | RTS1# | GPIO | 36 | GPO | LVDS_VBI | | | High |
| LB0LAT | WU7 | | GPIO | 17 | GPO | WLAR_ON | | | High |
| | | | GPIO | 20 | GPO | AMP_MUTE# | | | Low |
| PS2CLK0 | CECMU48 | TMR0 | GPIO | 85 | GPI | PANEL_VCC0# | | | |
| PS2DAT0 | WU48 | TMR1 | GPIO | 86 | GPO | PCH_PWRON | | Pull-down 10K to GND | High |
| PS2CLK1 | WU50 | OTR0# | GPIO | 87 | GPO | BT_ON | | Pull-up 100K to +3.3V, Pull-down 100K to GND | High |
| PS2DAT1 | WU51 | RTS0# | GPIO | 88 | GPI | Q_4m1 | | Pull-up 10K to +3.3V | |
| PS2CLK2 | WU52 | | GPIO | 89 | GPO | TP_CLK | | Pull-up 4.7K to +3.3V(IN) | |
| PS2DAT2 | WU51 | | GPIO | 90 | GPO | TP_DATA | | Pull-up 4.7K to +3.3V(IN) | |
| SMCLK2 | WU52 | PEQ | GPIO | 117 | PEQ | EC_PEQ | | | |
| SMDAT2 | WU53 | RECROT# | GPIO | 118 | GPO | REUL_ON | | | High |
| | | | GPIO | 106 | GPO | ID_DET | | Pull-up 100K to +3.3V | High |
| FDI02 | WU68 | DIR1/HSBUSY | GPIO | 107 | GPO | SW_release | | | High |
| | WU69 | SSCE0# | GPIO | 100 | GPO | CHUCORE_ON | | | High |
| | WU70 | DSR0# | GPIO | 104 | x | NVDD_EN | | | |
| CLKRUN# | WU15 | SR1/SMCLK3 | GPIO | 93 | CLKRUN# | PM_CLKRUN# | | Pull-up 8.2K to +3.3V | Low |
| CRX1 | WU17 | SOUT1/SMDAT3 | GPIO | 94 | GPI | PCH_BL_EN | | Pull-down 100K to GND | High |
| CTX1 | WU18 | | GPIO | 95 | GPI | GP_APO | | Pull-up 1M to +3.3V | |
| HSCLK# | WU19 | | GPIO | 96 | HSCLK# | EC_HSC0W#(N) | | | |
| HSCK | WU40 | | GPIO | 97 | HSCK | EC_HSC0(N) | | | |
| HMS0 | WU41 | | GPIO | 98 | HMS0 | EC_HMS0(N) | | | |
| HMS2 | WU42 | | GPIO | 99 | HMS2 | EC_HMS2(N) | | | |
| ADC0 | WU71 | | GPIO | 66 | GPI | EC_OVERT# | | Pull-up 100K to +3.3V | Low |
| ADC1 | WU72 | | GPIO | 67 | GPI | 1.8V_MAIN_EN(N) | | | |
| ADC2 | WU73 | | GPIO | 68 | GPI | PCIE_WAKE#(N) | | | |
| ADC3 | WU74 | | GPIO | 69 | GPO | FAN_enable1 | | | High |
| ADC4 | WU28 | | GPIO | 70 | ADC4 | BAT_V | | | |
| ADC5 | WU29 | DCD1# | GPIO | 71 | ADC5 | BATT_TEMP | | Pull-up 20K to +3.3V | |
| ADC6 | WU30 | DSR1# | GPIO | 72 | ADC6 | Adapter_I bat | | | |
| ADC7 | WU31 | CTS1# | GPIO | 73 | ADC7 | BAT_V | | Pull-up 93.1K to BAT+, Pull-down 13.3K to GND | |
| HDIO2 | WU80 | TACH2 | GPIO | 76 | GPO | EC_BL_ON | | Pull-up 10K to +3.3V | High |
| HDIO3 | WU81 | | GPIO | 77 | GPO | EC_PROCHOT# | | | Low |
| DAC2 | WU82 | TACH0B | GPIO | 78 | DAC2 | FAN_CTRL0 | | | |
| DAC3 | WU83 | TACH1B | GPIO | 79 | TACH1B | FAN_SPD_DETECT2 | | | |
| DAC4 | WU84 | DCD0# | GPIO | 80 | DAC4 | FAN_CTRL1 | | | |
| DACS | WU85 | RG2# | GPIO | 81 | DACS | CHG_RBY | | | |
| CK32K | WU86 | RG2# | GPIO | 128 | x | x(Pin128/GND) | | | |
| CK32KE | | | GPIO | 2 | x | x(Pin2/GND) | | | |
| LAD0 | | | GPIO | 10 | LAD0 | LPC_AD0_EC | | | |
| LAD1 | | | GPIO | 9 | LAD1 | LPC_AD1_EC | | | |
| LAD2 | | | GPIO | 8 | LAD2 | LPC_AD2_EC | | | |
| LAD3 | | | GPIO | 7 | LAD3 | LPC_AD3_EC | | | |
| LPCCLK | | | GPIO | 13 | LPCCLK | CLK_EC_LPC | | | |
| LFRAME# | | | GPIO | 6 | LFRAME# | LPC_FRAME# | | | |
| SERR0 | | | GPIO | 5 | SERR0 | INT_SERR0 | | Pull-up 10K to +3.3V | |

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26 M_A_DQ0
26 M_A_DQ1
26 M_A_DQ2
26 M_A_DQ3
26 M_A_DQ4
26 M_A_DQ5
26 M_A_DQ6
26 M_A_DQ7
26 M_A_DQ8
26 M_A_DQ9
26 M_A_DQ10
26 M_A_DQ11
26 M_A_DQ12
26 M_A_DQ13
26 M_A_DQ14
26 M_A_DQ15
26 M_A_DQ16
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26 M_A_DQ61
26 M_A_DQ62
26 M_A_DQ63

BR6
BT6
BP3
BR3
BN5
BP6
BP2
BN3
BL4
BL5
BL2
BM1
BK4
BK5
BK1
BK2
BG4
BG5
BF4
BF5
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BF1
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BD2
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BC4
BC5
BD5
BD4
BC1
BC2
AB1
AB2
AA4
AA5
AB5
AB4
AA2
AA1
V5
V2
U1
U2
V1
V4
U5
U4
R2
P5
R4
P4
R5
P2
R1
P1
M4
M1
L4
L2
M5
M2
L5
L1
BA2
BA1
AY4
AY5
BA5
BA4
AY1
AY2

DDR CHANNEL A

@SKL_H_BGA_BGA
REV = 1

SKYLAKE_HA70
BGA1440

DDR0_DQ[0]
DDR0_DQ[1]
DDR0_DQ[2]
DDR0_DQ[3]
DDR0_DQ[4]
DDR0_DQ[5]
DDR0_DQ[6]
DDR0_DQ[7]
DDR0_DQ[8]
DDR0_DQ[9]
DDR0_DQ[10]
DDR0_DQ[11]
DDR0_DQ[12]
DDR0_DQ[13]
DDR0_DQ[14]
DDR0_DQ[15]
DDR0_DQ[16]/DDR0_DQ[32]
DDR0_DQ[17]/DDR0_DQ[33]
DDR0_DQ[18]/DDR0_DQ[34]
DDR0_DQ[19]/DDR0_DQ[35]
DDR0_DQ[20]/DDR0_DQ[36]
DDR0_DQ[21]/DDR0_DQ[37]
DDR0_DQ[22]/DDR0_DQ[38]
DDR0_DQ[23]/DDR0_DQ[39]
DDR0_DQ[24]/DDR0_DQ[40]
DDR0_DQ[25]/DDR0_DQ[41]
DDR0_DQ[26]/DDR0_DQ[42]
DDR0_DQ[27]/DDR0_DQ[43]
DDR0_DQ[28]/DDR0_DQ[44]
DDR0_DQ[29]/DDR0_DQ[45]
DDR0_DQ[30]/DDR0_DQ[46]
DDR0_DQ[31]/DDR0_DQ[47]
DDR0_DQ[32]/DDR1_DQ[0]
DDR0_DQ[33]/DDR1_DQ[1]
DDR0_DQ[34]/DDR1_DQ[2]
DDR0_DQ[35]/DDR1_DQ[3]
DDR0_DQ[36]/DDR1_DQ[4]
DDR0_DQ[37]/DDR1_DQ[5]
DDR0_DQ[38]/DDR1_DQ[6]
DDR0_DQ[39]/DDR1_DQ[7]
DDR0_DQ[40]/DDR1_DQ[8]
DDR0_DQ[41]/DDR1_DQ[9]
DDR0_DQ[42]/DDR1_DQ[10]
DDR0_DQ[43]/DDR1_DQ[11]
DDR0_DQ[44]/DDR1_DQ[12]
DDR0_DQ[45]/DDR1_DQ[13]
DDR0_DQ[46]/DDR1_DQ[14]
DDR0_DQ[47]/DDR1_DQ[15]
DDR0_DQ[48]/DDR1_DQ[32]
DDR0_DQ[49]/DDR1_DQ[33]
DDR0_DQ[50]/DDR1_DQ[34]
DDR0_DQ[51]/DDR1_DQ[35]
DDR0_DQ[52]/DDR1_DQ[36]
DDR0_DQ[53]/DDR1_DQ[37]
DDR0_DQ[54]/DDR1_DQ[38]
DDR0_DQ[55]/DDR1_DQ[39]
DDR0_DQ[56]/DDR1_DQ[40]
DDR0_DQ[57]/DDR1_DQ[41]
DDR0_DQ[58]/DDR1_DQ[42]
DDR0_DQ[59]/DDR1_DQ[43]
DDR0_DQ[60]/DDR1_DQ[44]
DDR0_DQ[61]/DDR1_DQ[45]
DDR0_DQ[62]/DDR1_DQ[46]
DDR0_DQ[63]/DDR1_DQ[47]
DDR0_ECC[0]
DDR0_ECC[1]
DDR0_ECC[2]
DDR0_ECC[3]
DDR0_ECC[4]
DDR0_ECC[5]
DDR0_ECC[6]
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DDR0_CLKP[3]
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DDR0_CS#[3]
DDR0_ODT[0]
DDR0_ODT[1]
DDR0_ODT[2]
DDR0_ODT[3]
DDR0_BA[0]/DDR0_CAB[4]/DDR0_BA[0]
DDR0_BA[1]/DDR0_CAB[6]/DDR0_BA[1]
DDR0_BA[2]/DDR0_CAA[5]/DDR0_BG[0]
DDR0_RAS#/DDR0_CAB[3]/DDR0_MA[16]
DDR0_WE#/DDR0_CAB[2]/DDR0_MA[14]
DDR0_CAS#/DDR0_CAB[1]/DDR0_MA[15]
DDR0_MA[0]/DDR0_CAB[9]/DDR0_MA[0]
DDR0_MA[1]/DDR0_CAB[8]/DDR0_MA[1]
DDR0_MA[2]/DDR0_CAB[5]/DDR0_MA[2]
DDR0_MA[3]
DDR0_MA[4]
DDR0_MA[5]/DDR0_CAA[0]/DDR0_MA[5]
DDR0_MA[6]/DDR0_CAA[2]/DDR0_MA[6]
DDR0_MA[7]/DDR0_CAA[4]/DDR0_MA[7]
DDR0_MA[8]/DDR0_CAA[3]/DDR0_MA[8]
DDR0_MA[9]/DDR0_CAA[1]/DDR0_MA[9]
DDR0_MA[10]/DDR0_CAB[7]/DDR0_MA[10]
DDR0_MA[11]/DDR0_CAA[7]/DDR0_MA[11]
DDR0_MA[12]/DDR0_CAA[6]/DDR0_MA[12]
DDR0_MA[13]/DDR0_CAB[0]/DDR0_MA[13]
DDR0_MA[14]/DDR0_CAA[9]/DDR0_BG[1]
DDR0_MA[15]/DDR0_CAA[8]/DDR0_ACT#
DDR0_PAR
DDR0_ALERT#
DDR0_DQSN[0]
DDR0_DQSN[1]
DDR0_DQSN[2]/DDR0_DQSN[4]
DDR0_DQSN[3]/DDR0_DQSN[5]
DDR0_DQSP[4]/DDR1_DQSP[0]
DDR0_DQSP[5]/DDR1_DQSP[1]
DDR0_DQSP[6]/DDR1_DQSP[4]
DDR0_DQSP[7]/DDR1_DQSP[5]
DDR0_DQSP[0]
DDR0_DQSP[1]
DDR0_DQSP[2]/DDR0_DQSP[4]
DDR0_DQSP[3]/DDR0_DQSP[5]
DDR0_DQSN[4]/DDR1_DQSN[0]
DDR0_DQSN[5]/DDR1_DQSN[1]
DDR0_DQSN[6]/DDR1_DQSN[4]
DDR0_DQSN[7]/DDR1_DQSN[5]
DDR0_DQSP[8]
DDR0_DQSN[8]

AG1
AG2
AK1
AK2
AL3
AK3
AL2
AL1
AT1
AT2
AT3
AT5
AD5
AE2
AD2
AE5
AD3
AE4
AE1
AD4
AH5
AH1
AU1
AH4
AG4
AD1
AH3
AP4
AN4
AP5
AP2
AP1
AP3
AN1
AN3
AT4
AH2
AN2
AU4
AE3
AU2
AU3
AG3
AU5
BR5
BL3
BG3
BD3
AB3
V3
R3
M3
BP5
BK3
BF3
BC3
AA3
U3
P3
L3
AY3
BA3

Correct CLK1 P/N
Sun 12/9

MA_CLK0 26
MA_CLK#0 26
MA_CLK#1 26
MA_CLK1 26

change DDR0_CKP/N(2,3) to (1,0)

MA_CKE0 26
MA_CKE1 26

change DDR0_CKE(2,3) to (1,0)

MA_CS#0 26
MA_CS#1 26

change DDR0_CS#(2,3) to (1,0)

MA_ODT0 26
MA_ODT1 26

change DDR0_ODT(2,3) to (1,0)

NPI modify---Leon 11/27

M_A_BA0 26
M_A_BA1 26
M_A_BG0 26
M_A_A16_MA_RAS# 26
M_A_A14_MA_WE# 26
M_A_A15_MA_CAS# 26

M_A_A0 26
M_A_A1 26
M_A_A2 26
M_A_A3 26
M_A_A4 26
M_A_A5 26
M_A_A6 26
M_A_A7 26
M_A_A8 26
M_A_A9 26
M_A_A10_AP 26
M_A_A11 26
M_A_A12 26
M_A_A13 26
M_A_BG1 26
M_A_ACT_N 26

DDR0_A_PARITY 26
DDR0_A_ALERT_N 26

M_A_DQS#0 26
M_A_DQS#1 26
M_A_DQS#2 26
M_A_DQS#3 26
M_A_DQS4 26
M_A_DQS5 26
M_A_DQS6 26
M_A_DQS7 26

M_A_DQS0 26
M_A_DQS1 26
M_A_DQS2 26
M_A_DQS3 26
M_A_DQS#4 26
M_A_DQS#5 26
M_A_DQS#6 26
M_A_DQS#7 26

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TEL:886-2-7718888 FAX:886-2-77218668

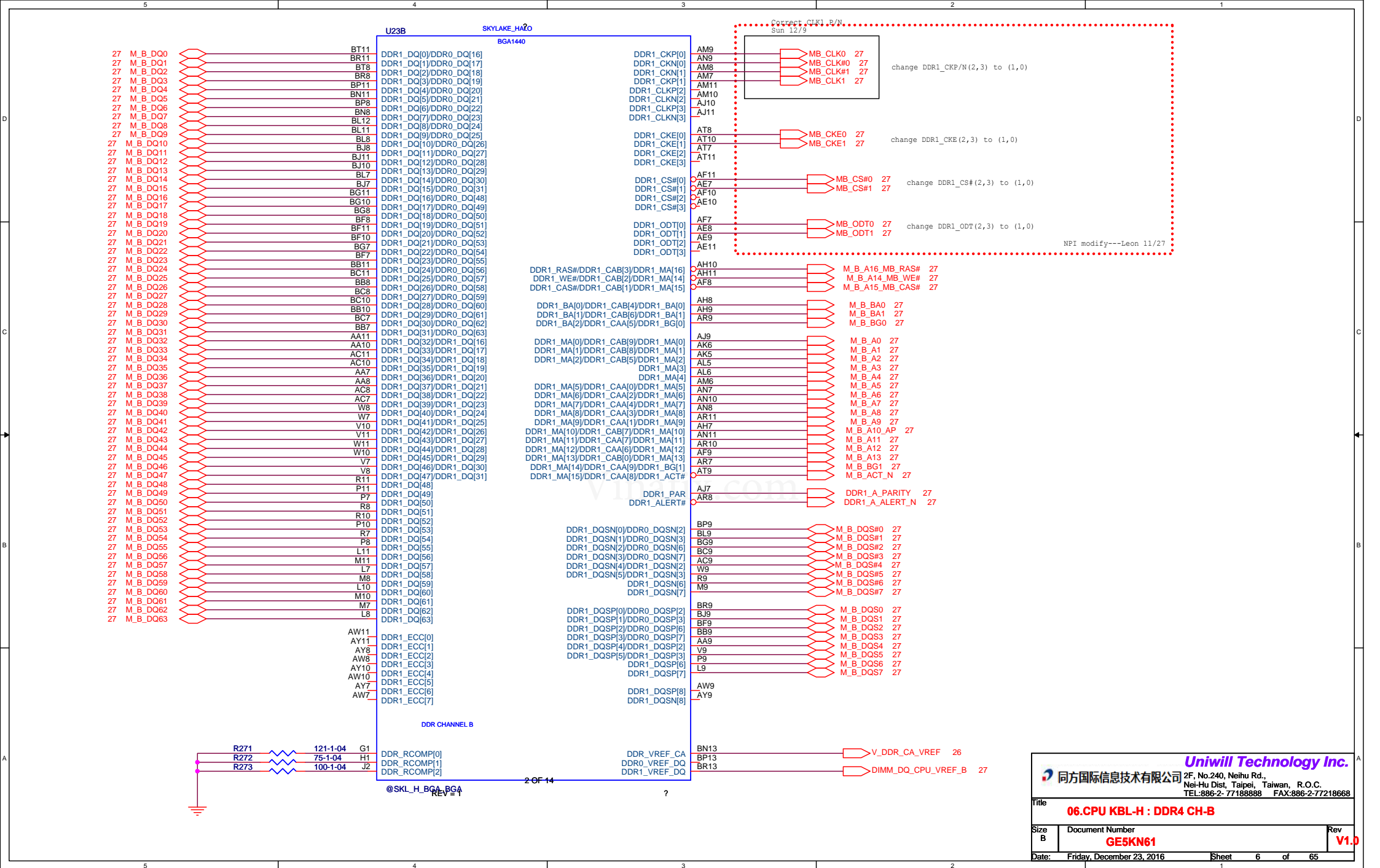
同方国际信息技术有限公司

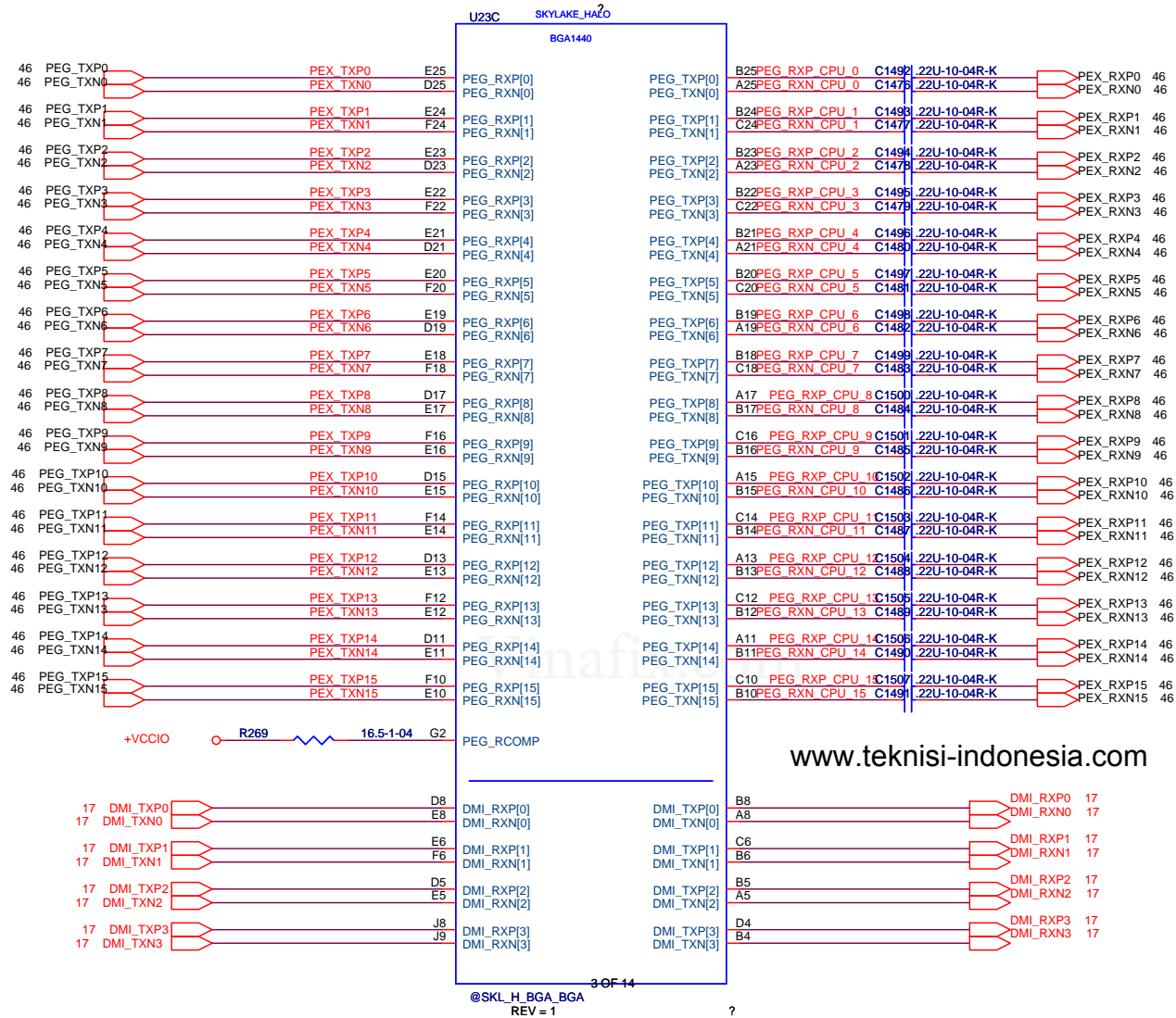
Title
05.CPU KBL-H : DDR4 CH-A

Size B Document Number
GE5KN61

Date: Friday, December 23, 2016 Sheet 5 of 65

Rev V1.0

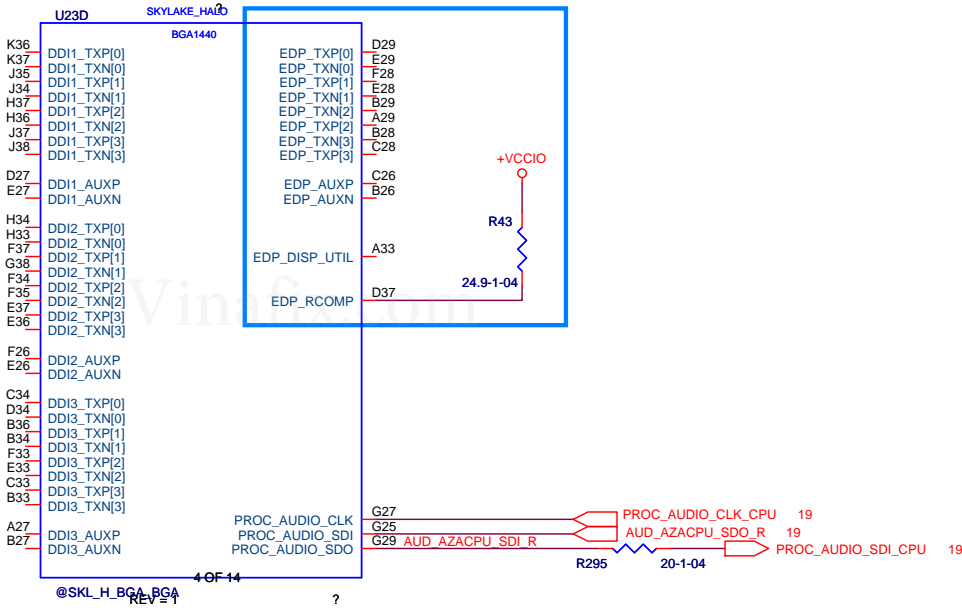


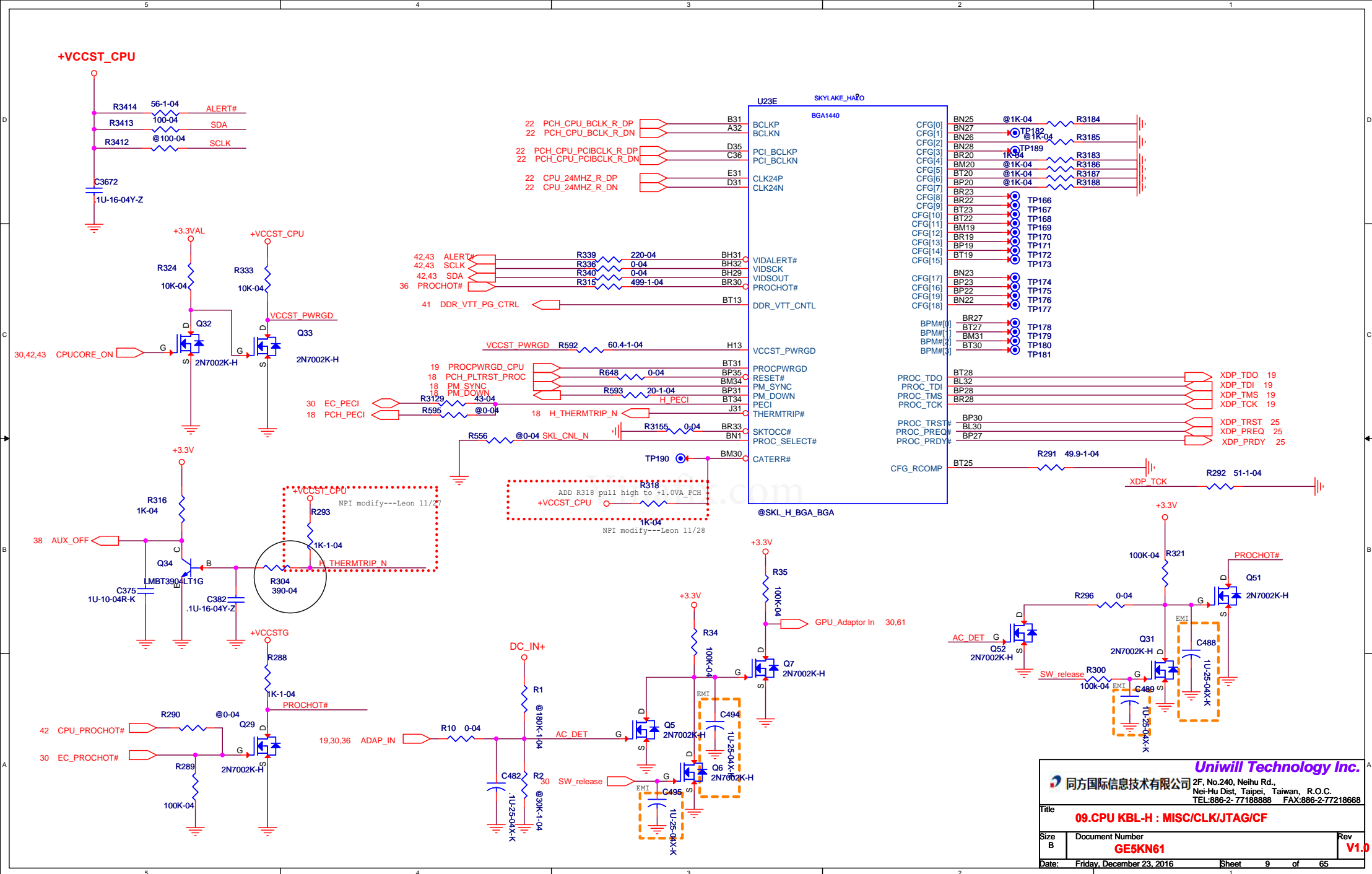


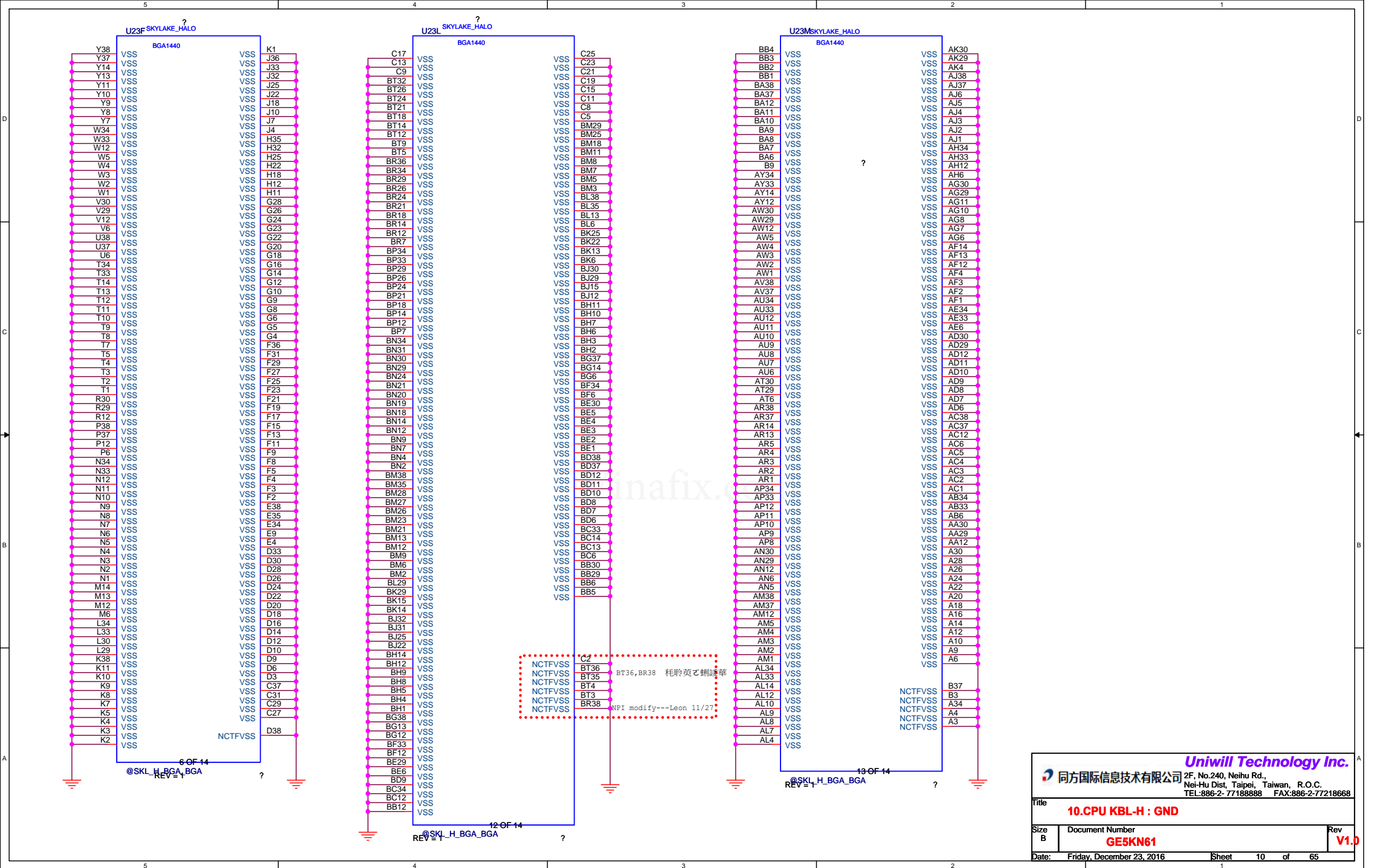
6.5.2 eDP* Disabling and Termination Guidelines

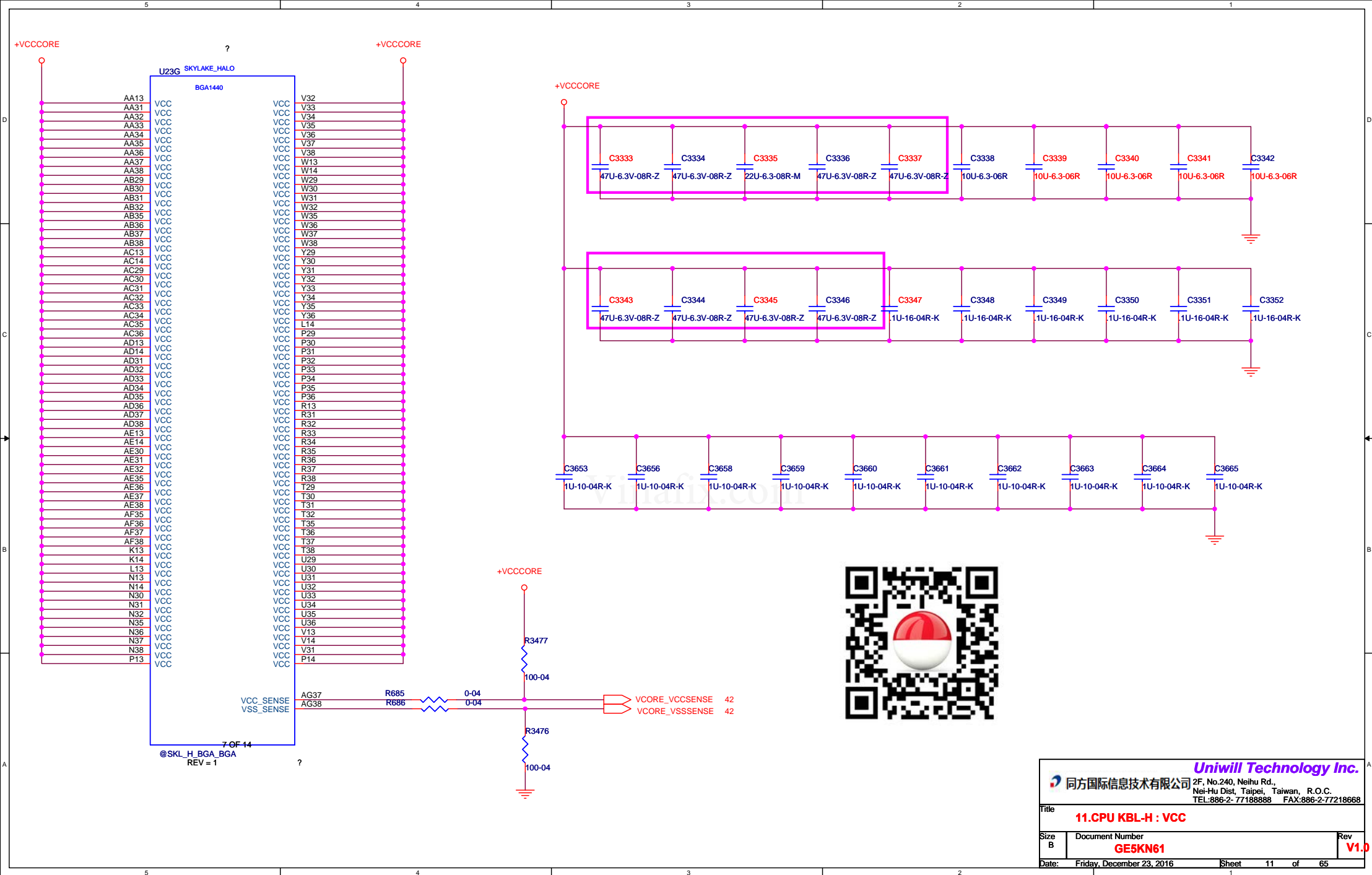
Table 6-11. eDP* Disabling and Termination Guidelines

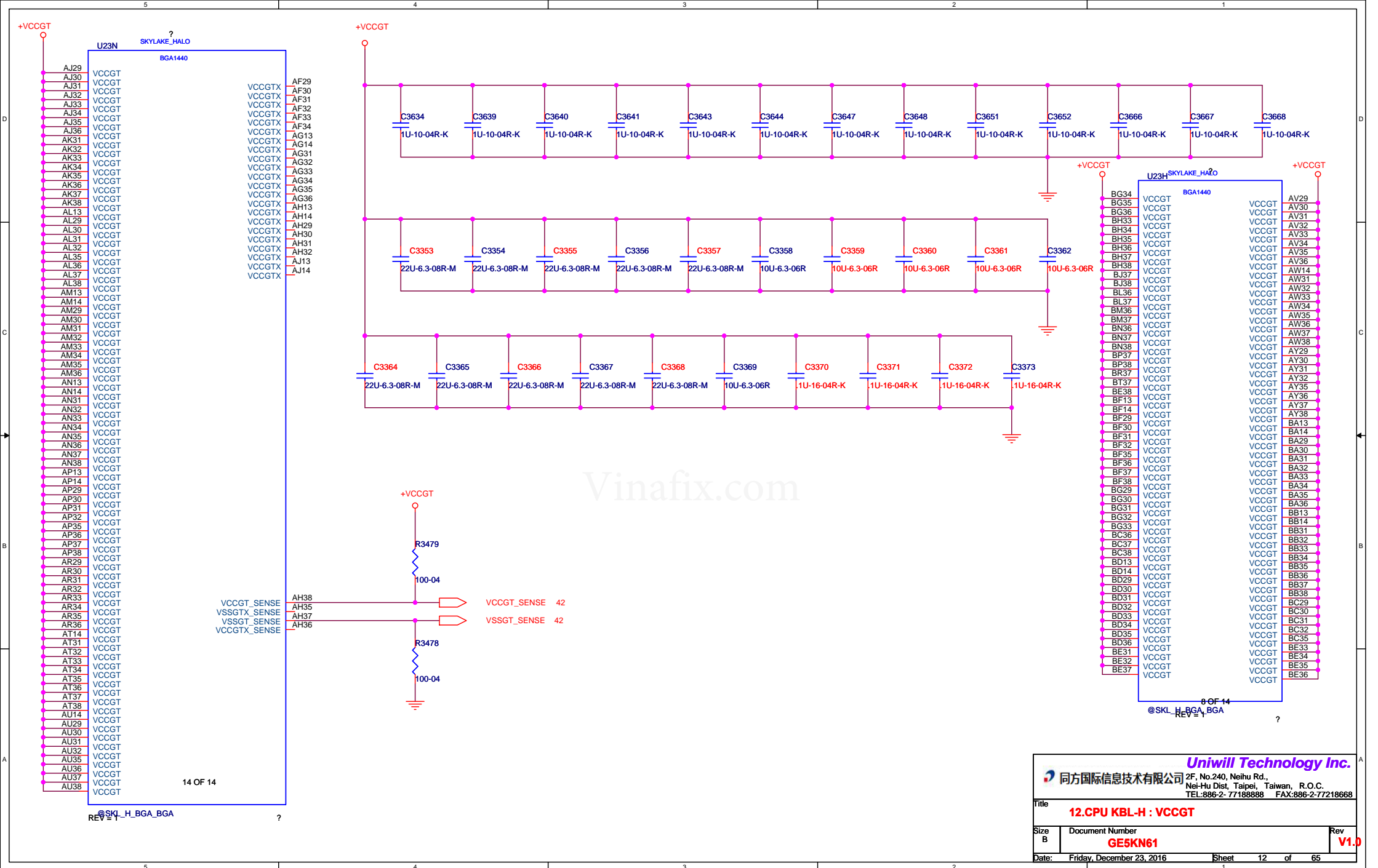
| Pin name | Recommendation |
|----------------|---|
| eDP_TXN/P[3:0] | No connect |
| EDP_AUXN/P | No connect |
| eDP_HPD | Pull down to ground via 100k ohm resistor |
| EDP_RCOMP | Pull up to VCCIO via 24.9 ohm resistor |
| eDP_DISP_UTIL | No connect |

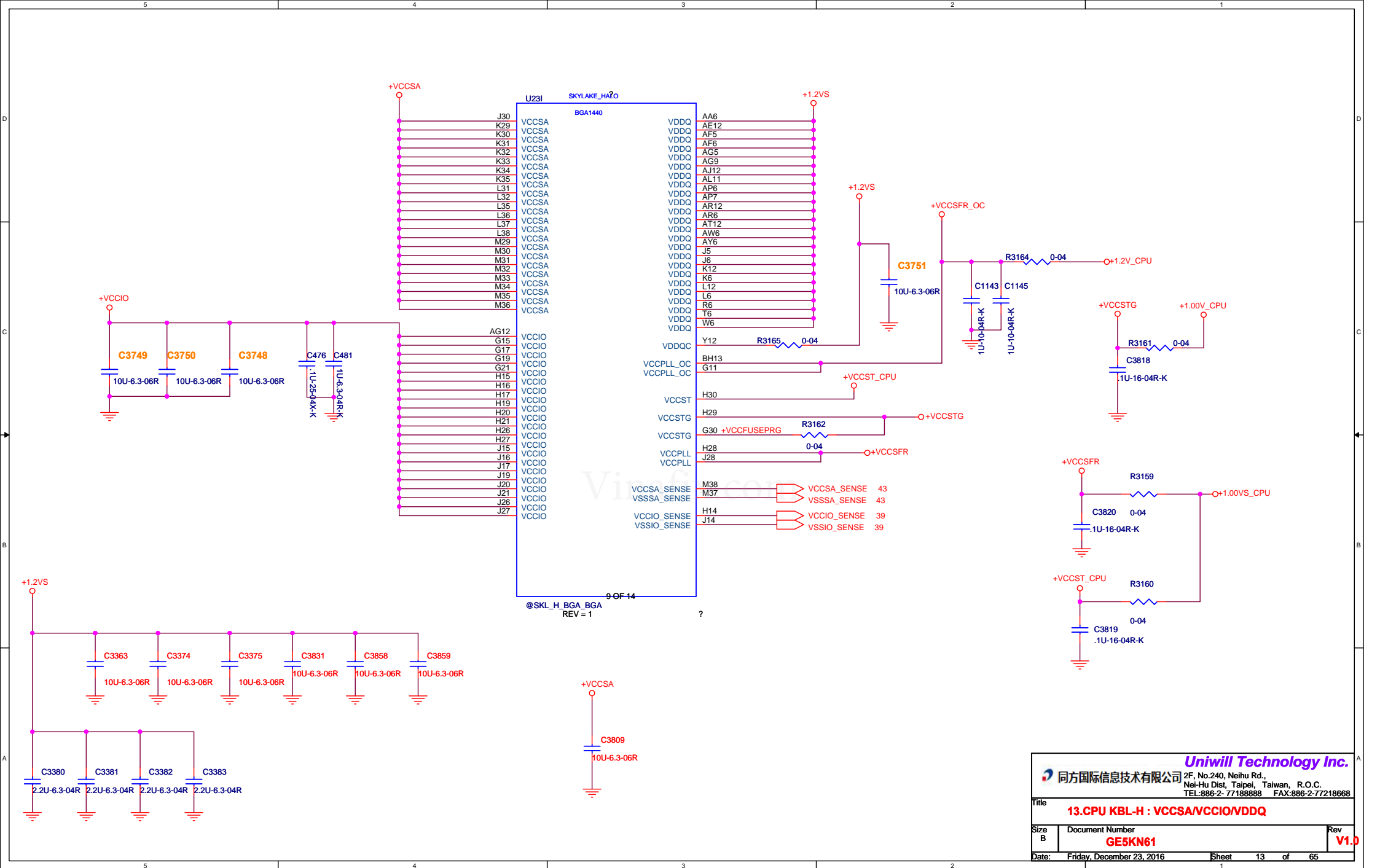




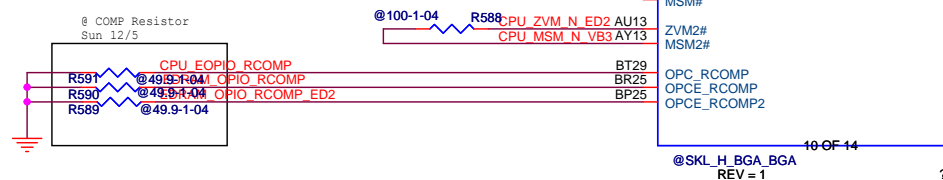




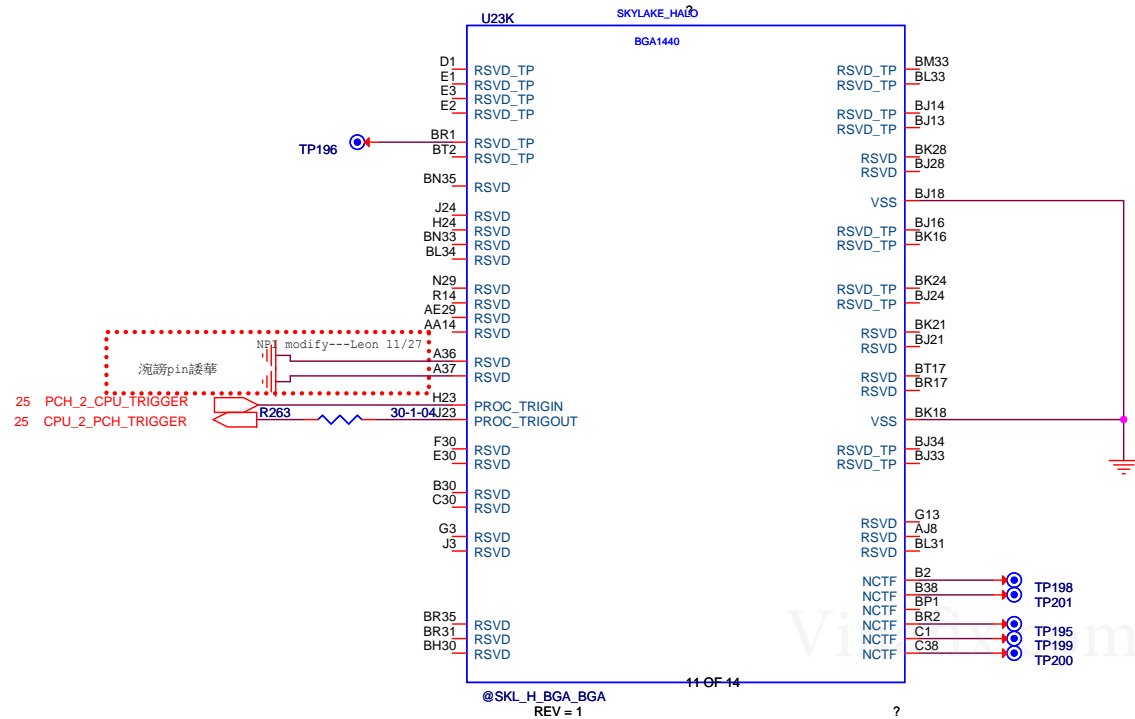


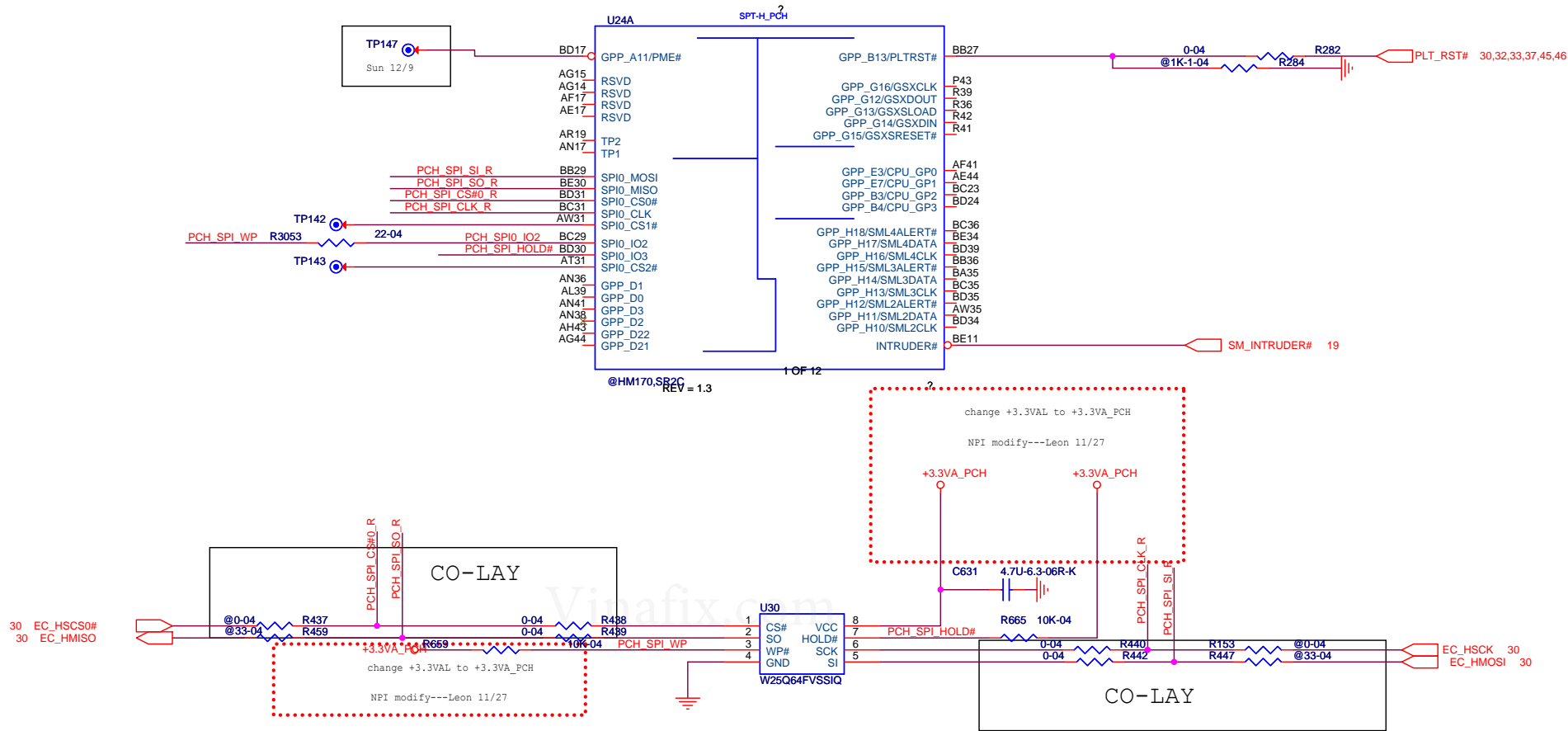


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| | | |
|--|---------------------------|----------------|
| Uniwill Technology Inc. | | |
| 2F, No.240, NeiHu Rd., Nei-Hu Dist, Taipei, Taiwan, R.O.C. TEL:886-2-77188888 FAX:886-2-77218668 | | |
| Title | | |
| 14.CPU KBL-H : VCCOPC/RSVD | | |
| Size | Document Number | Rev |
| B | GE5KN61 | V1.0 |
| Date: | Friday, December 23, 2016 | Sheet 14 of 65 |



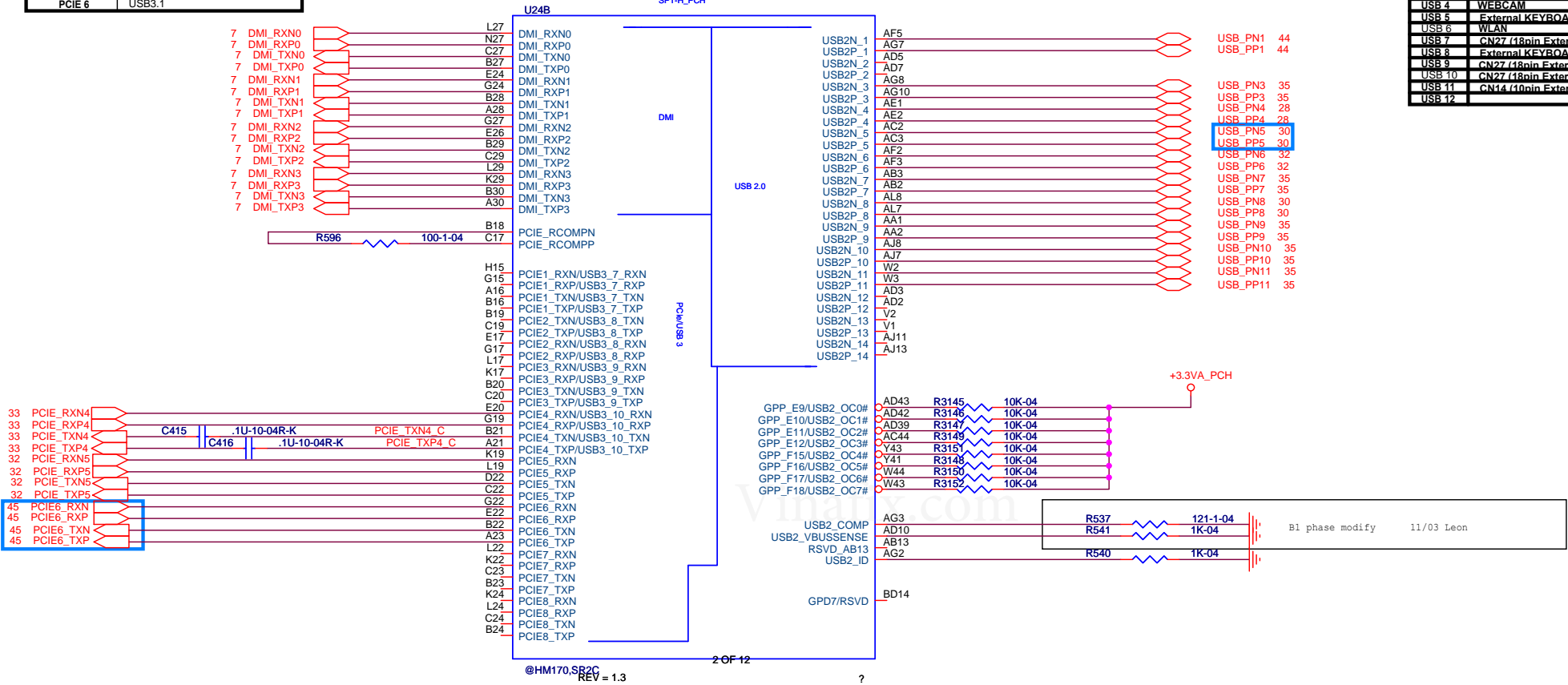


BBS_BIT0 - BIOS BOOT STRAP BIT 0

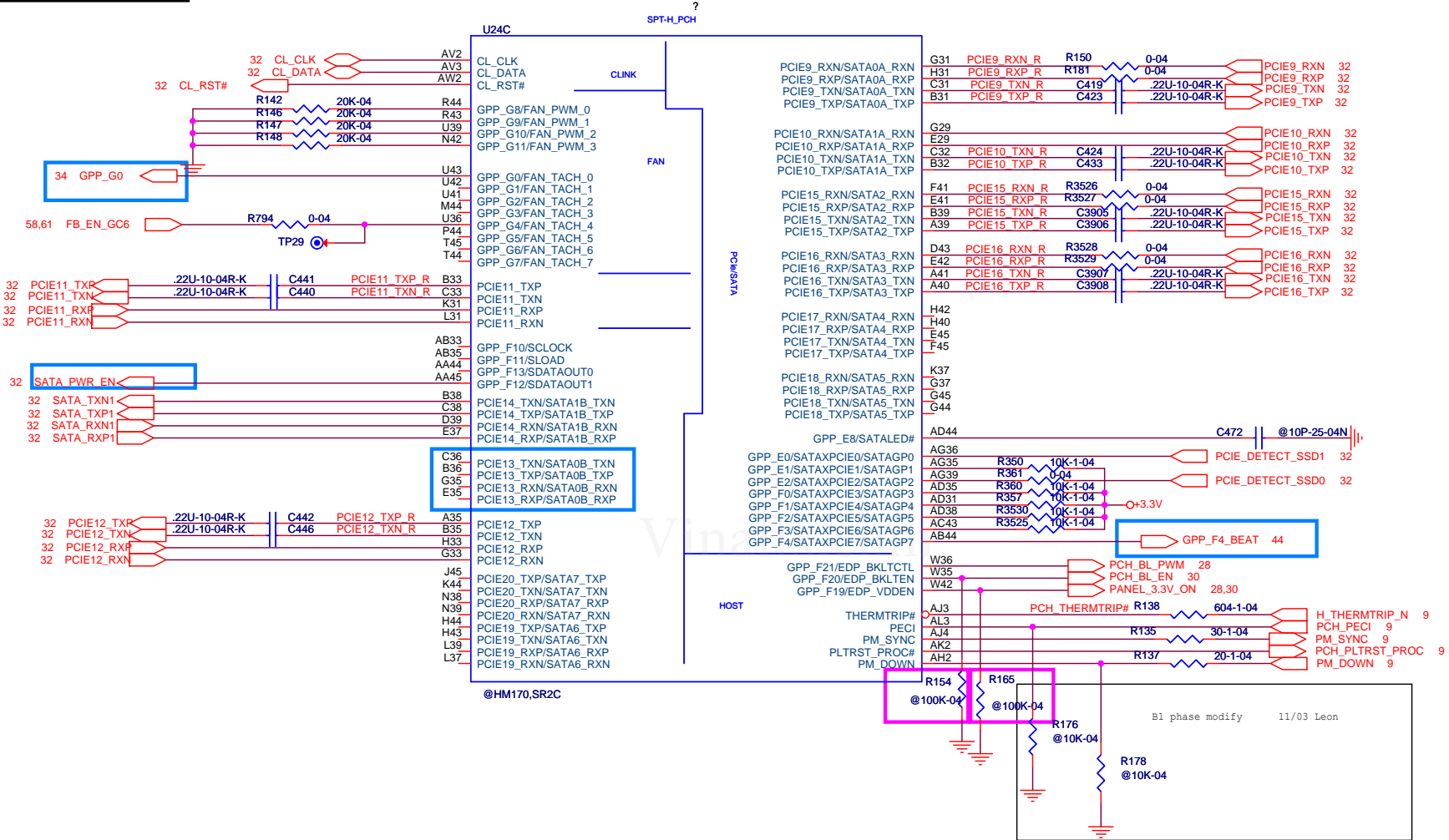
| BOOT BIOS STRAP | | |
|-----------------|----------|--------------------|
| BBS_BIT1 | BBS_BIT0 | BOOT BIOS LOCATION |
| 0 | 0 | LPC |
| 0 | 1 | RESERVED(NAND) |
| 1 | 0 | --- |
| 1 | 1 | SPI |

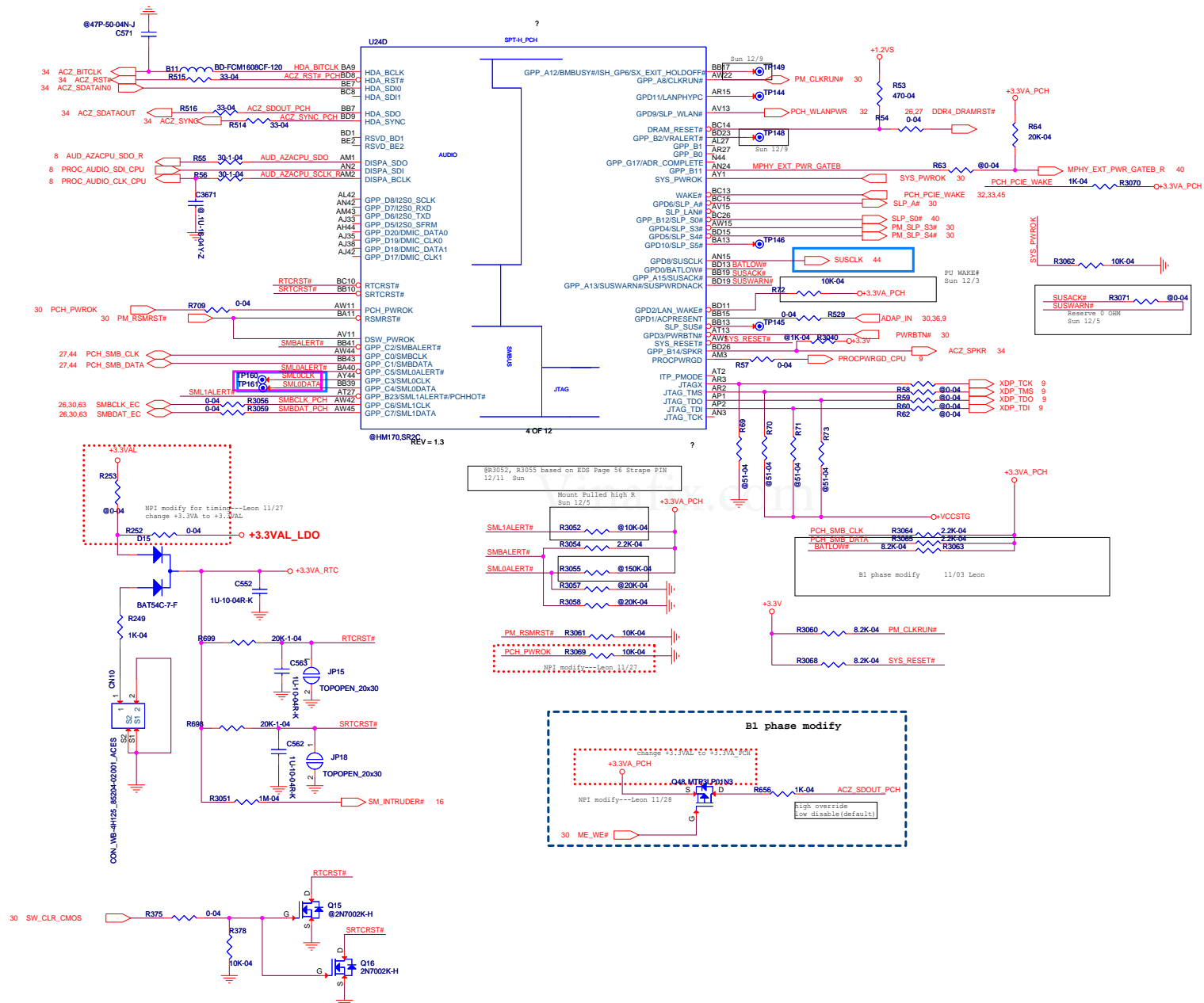
| PCIE | Location |
|--------|----------|
| PCIE 4 | LAN |
| PCIE 5 | WLAN |
| PCIE 6 | USB3.1 |

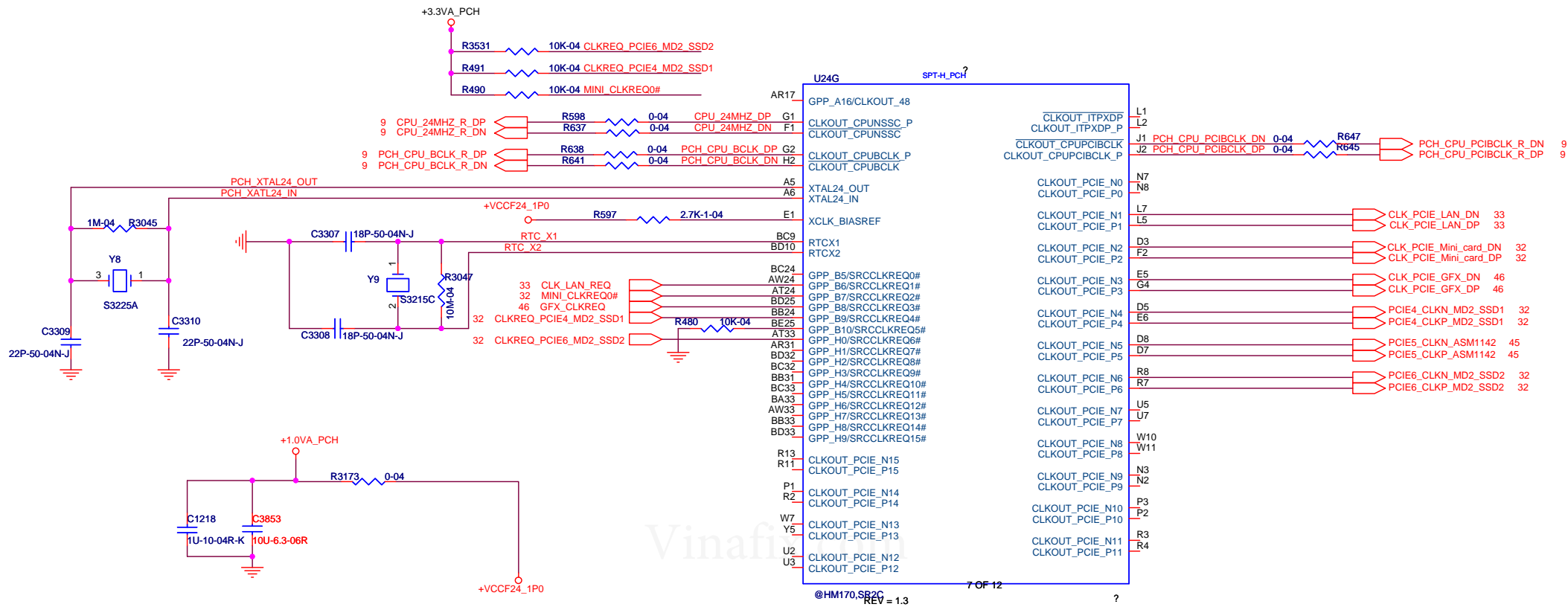
| USB | Location |
|--------|------------------------------|
| USB 1 | USB3.0 |
| USB 2 | USB3.0 |
| USB 3 | CN14 (10pin External USB BD) |
| USB 4 | WEBCAM |
| USB 5 | External KEYBOARD FOR 全尺寸 |
| USB 6 | WLAN |
| USB 7 | CN27 (18pin External USB BD) |
| USB 8 | External KEYBOARD |
| USB 9 | CN27 (18pin External USB BD) |
| USB 10 | CN27 (18pin External USB BD) |
| USB 11 | CN14 (10pin External USB BD) |
| USB 12 | |



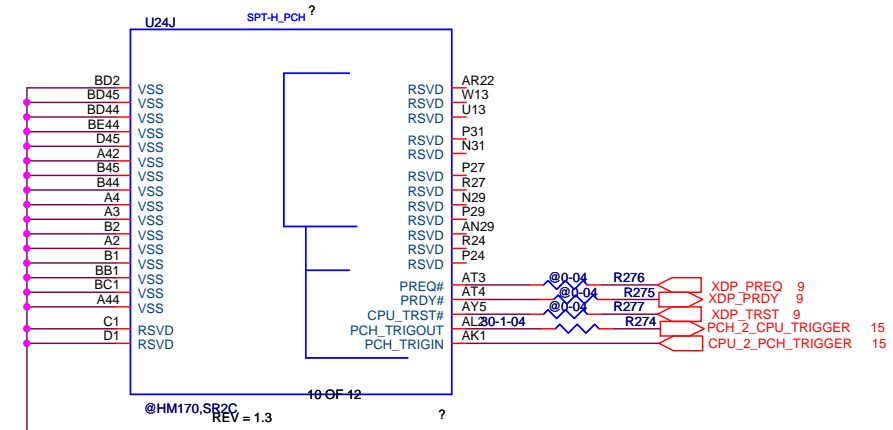
| PCIE | Location |
|-----------------|-----------------|
| PCIE 9,10,11,12 | PCIE(SATA) SSD1 |
| PCIE 14 | SATA HDD |
| PCIE 15,16 | PCIE(SATA) SSD2 |

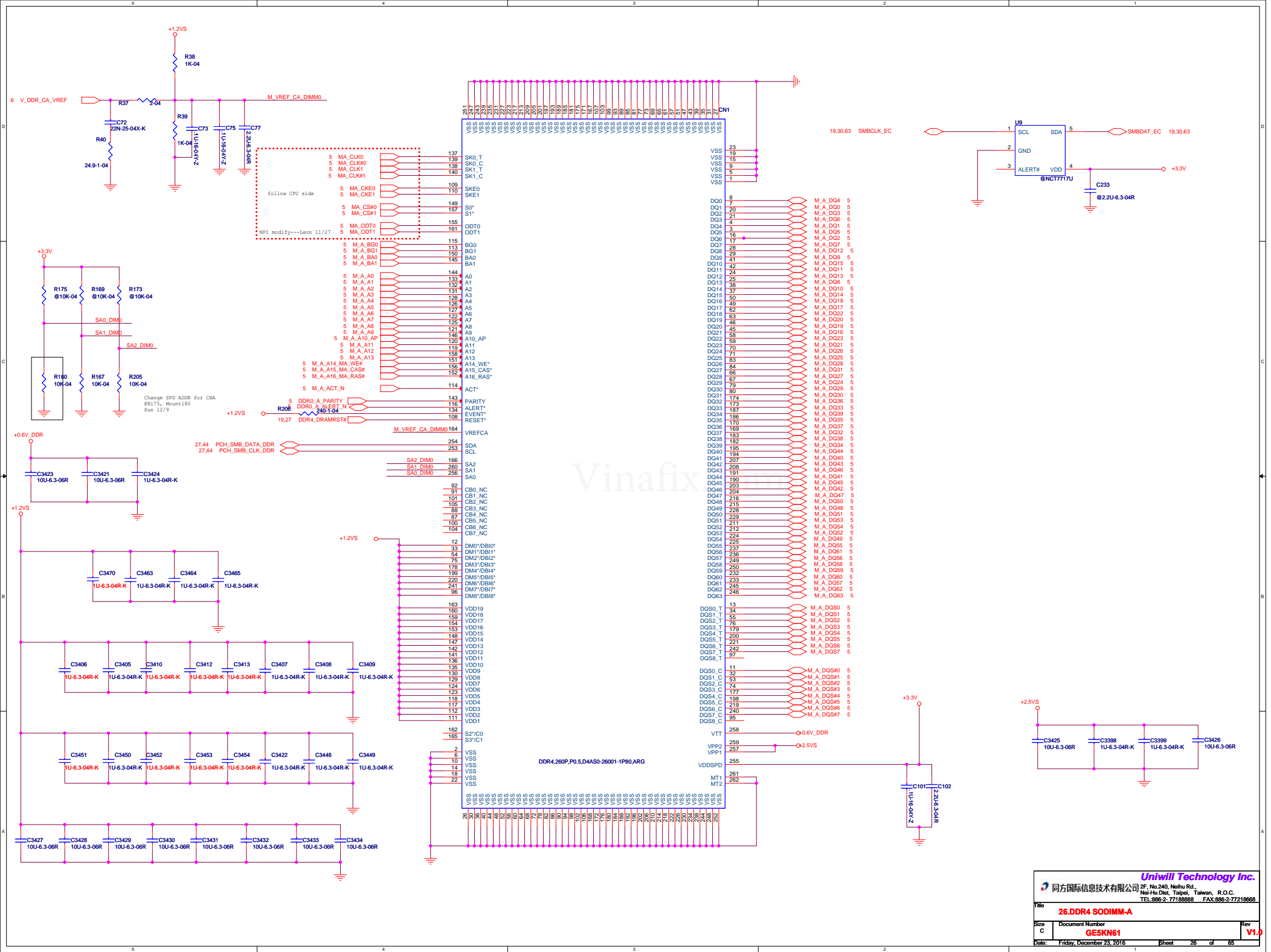


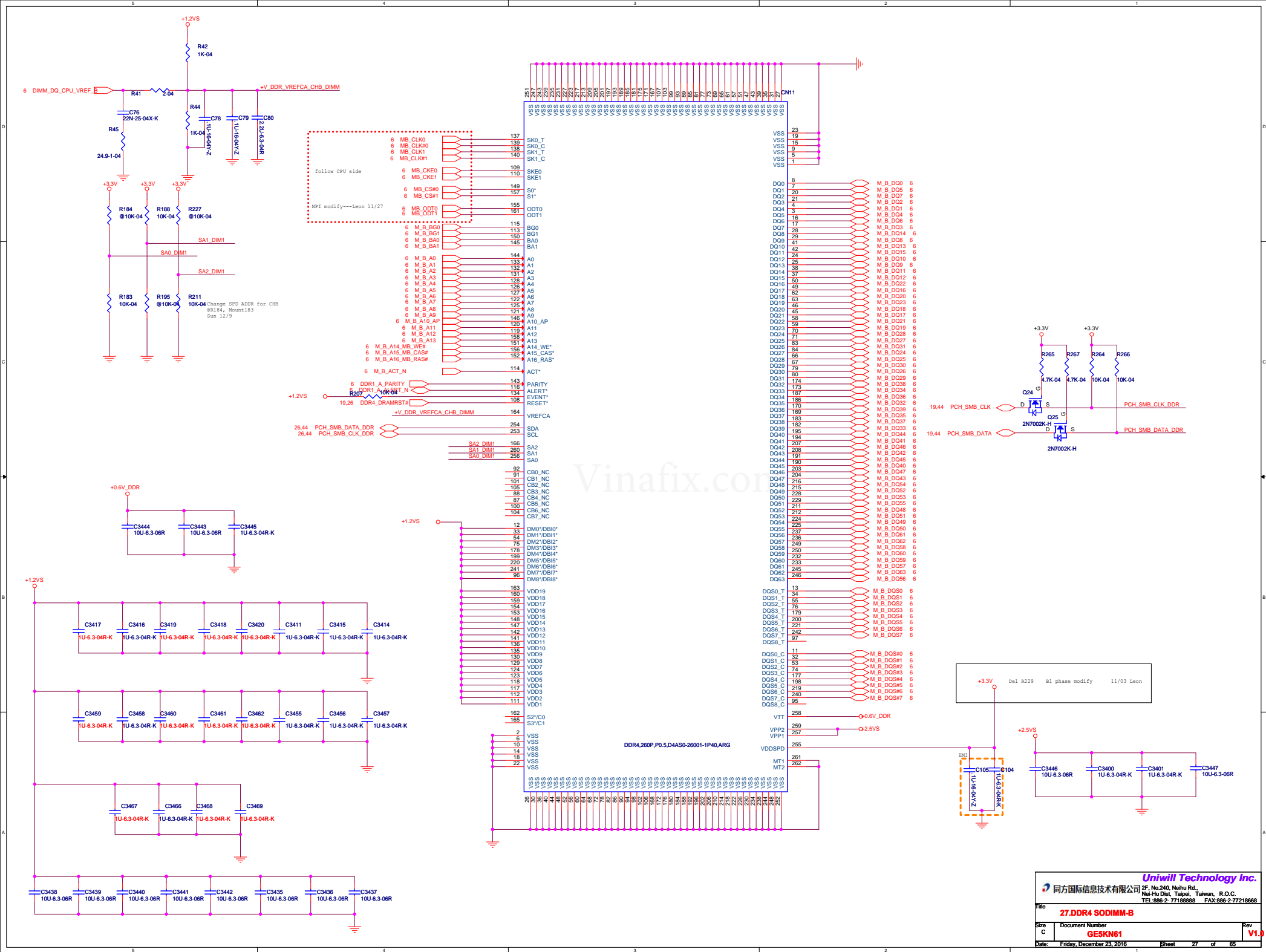


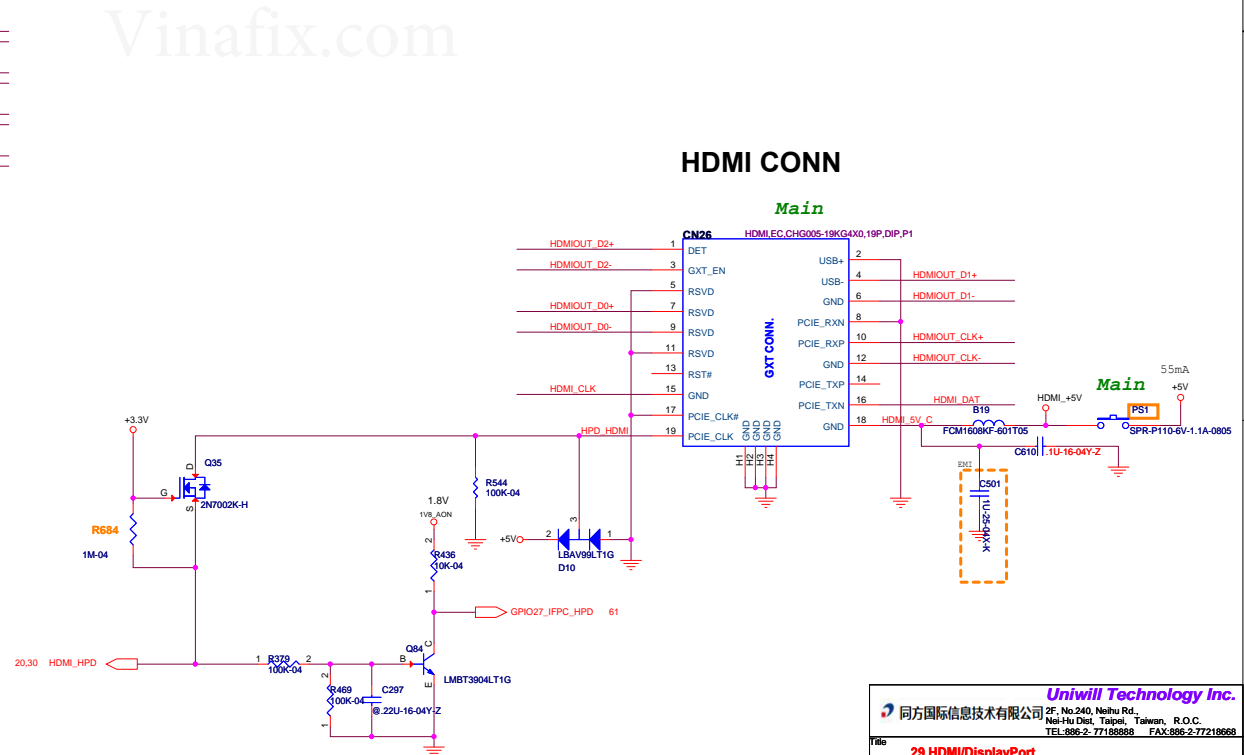
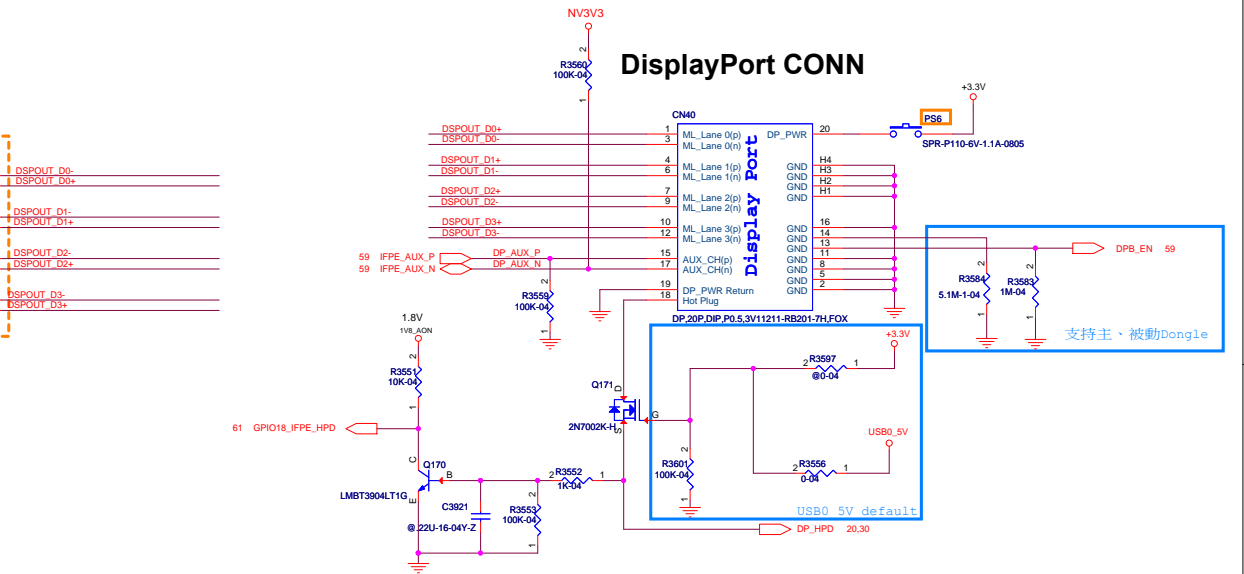
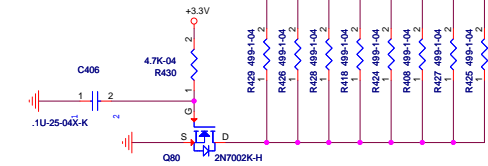






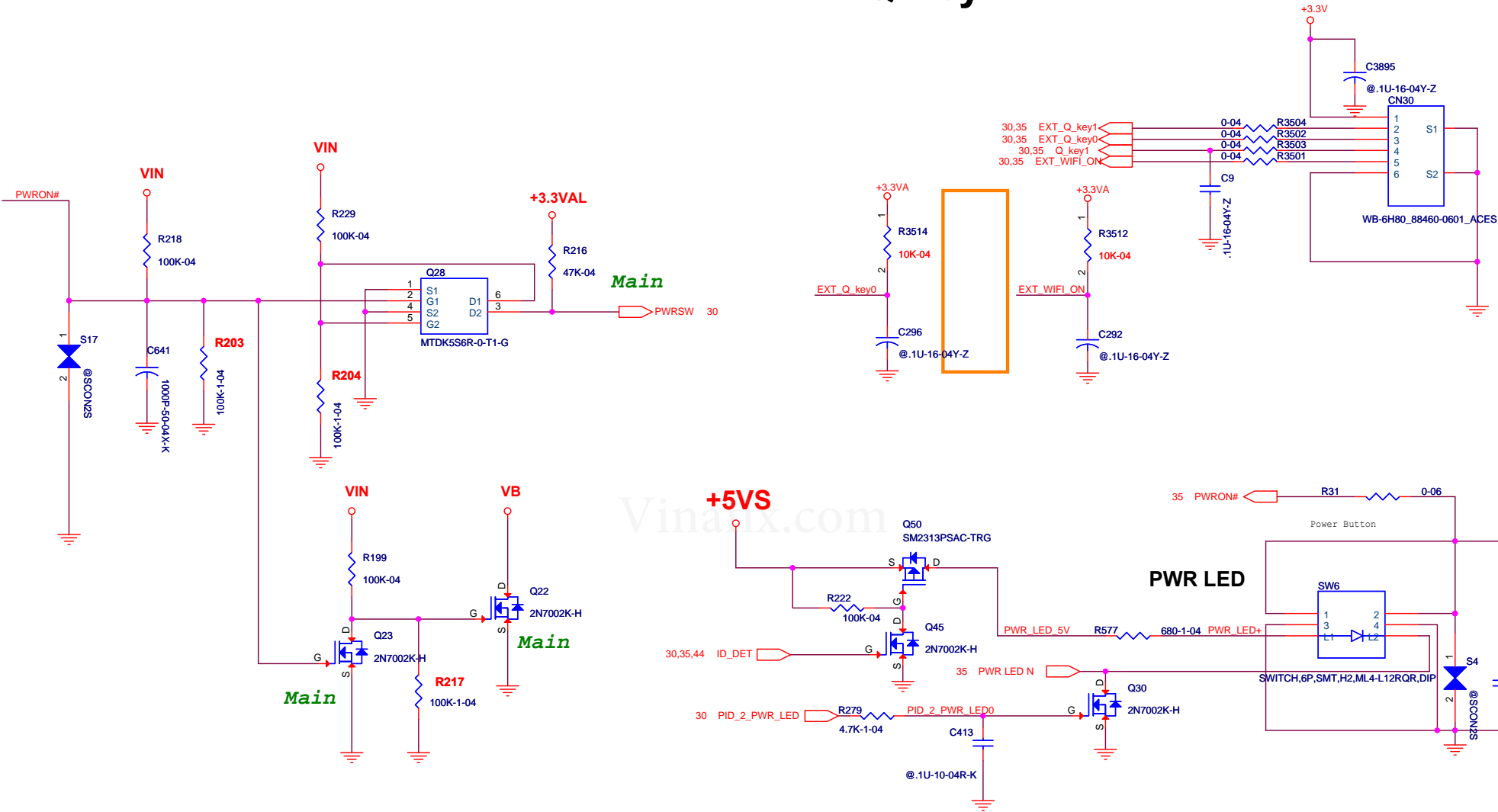




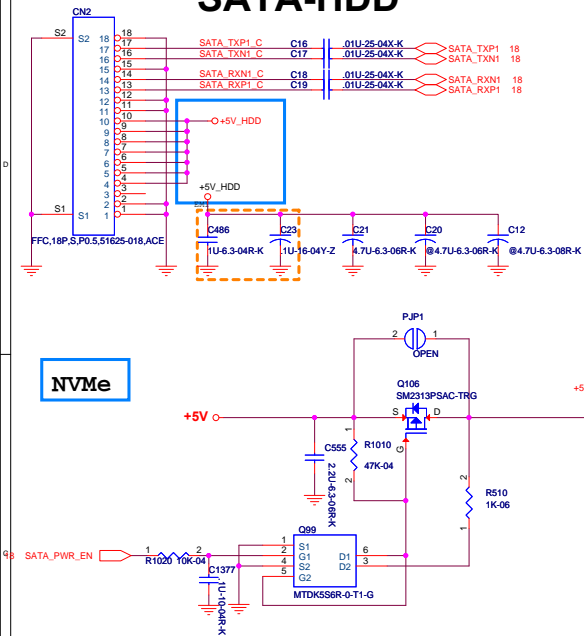


PWR SW

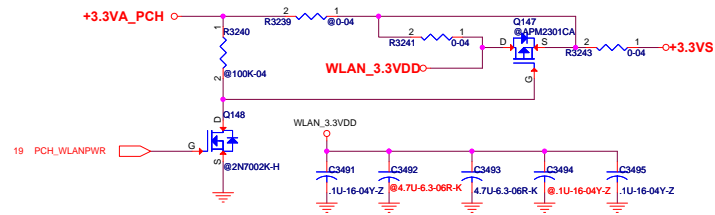
Q Key



SATA-HDD



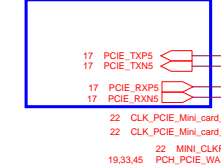
MINI CARD CONN



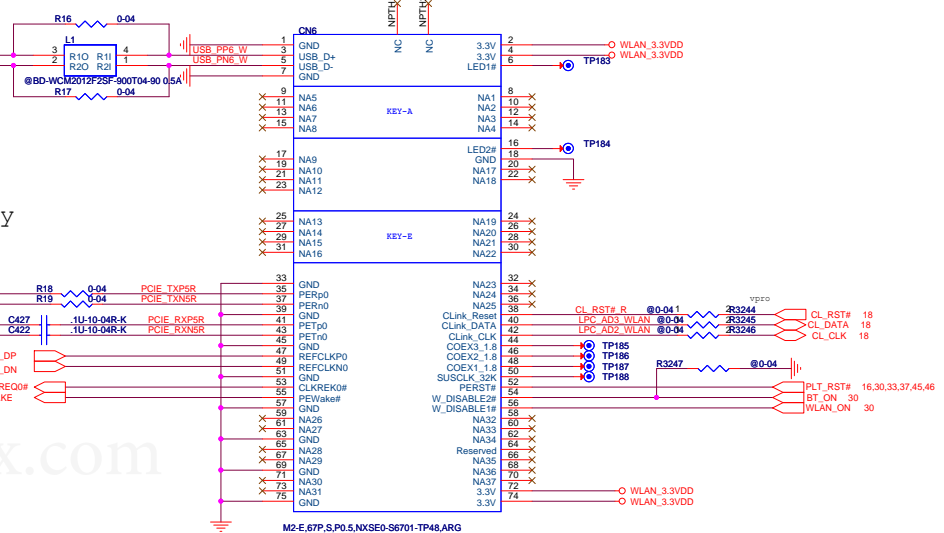
B phase modify



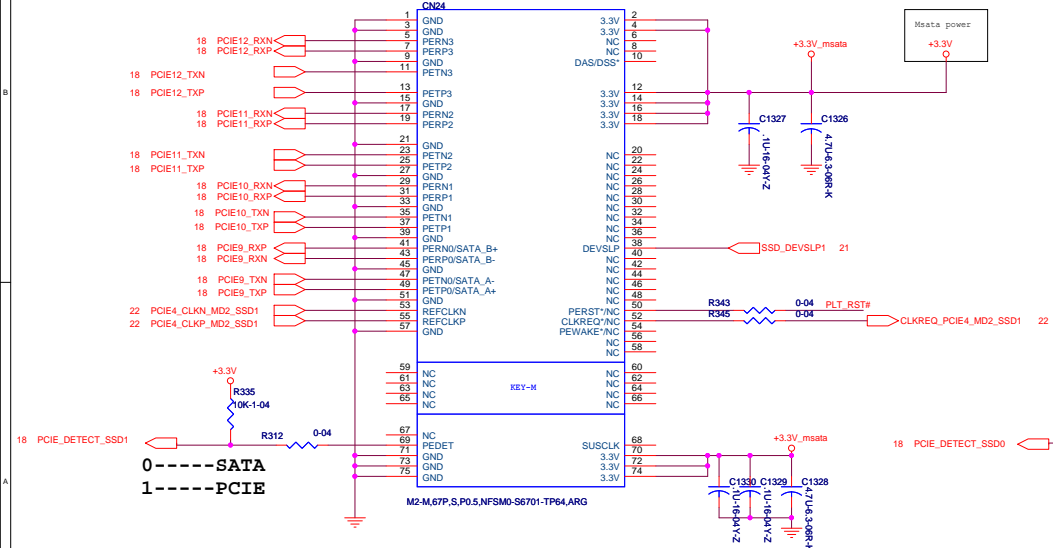
B phase modify



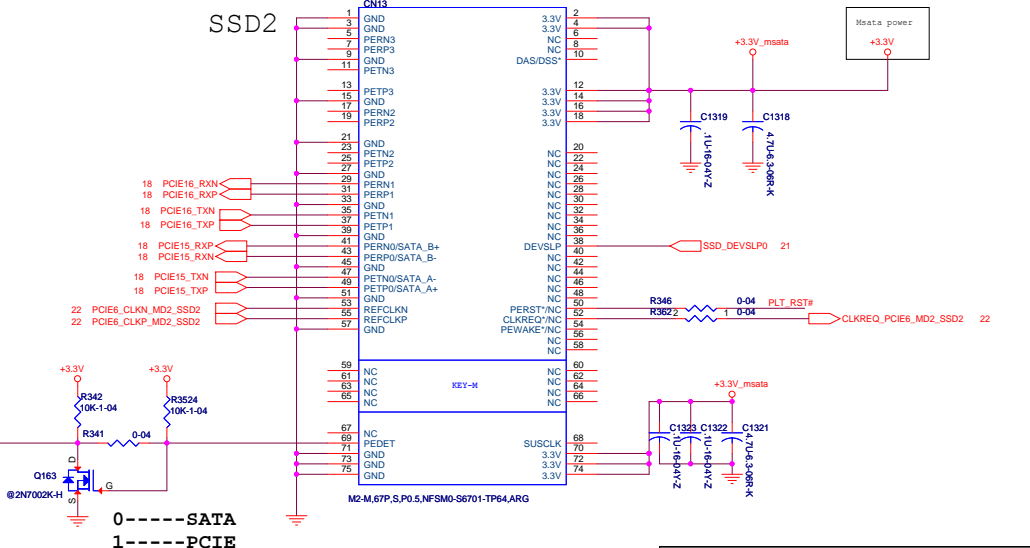
WLAN

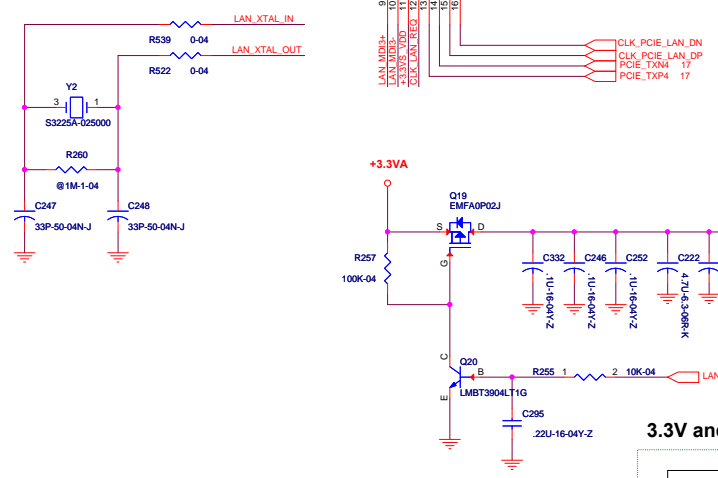
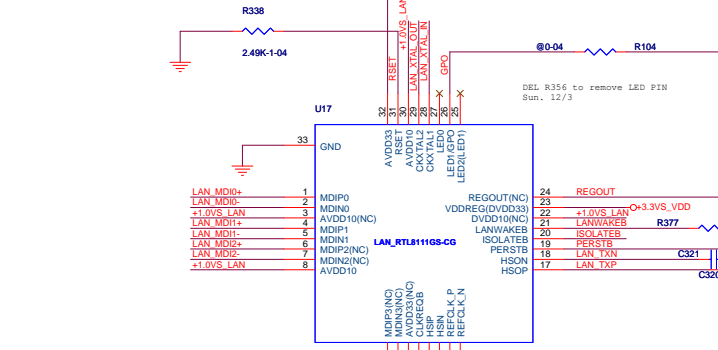
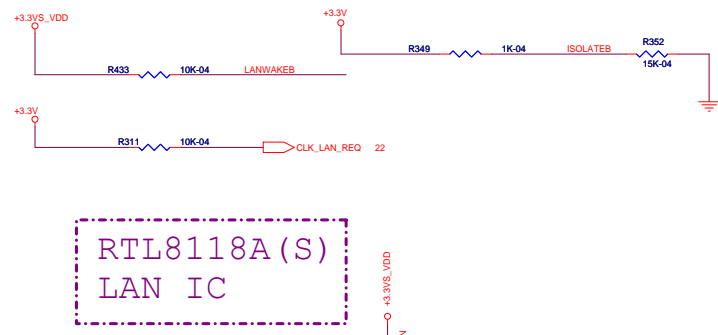


SSD1



SSD2





3.3V and 1.0V Power-Supply Configurations

| | 1.0 V source | Lx | Cout1,2 | Cin1,2 | R1 | C7 |
|--|--------------|----|---------|--------|----|----|
| RTL8111G Series/ RTL8111H Series/ RTL8107E Series | LDO | X | X | X | O | O |
| RTL8111G Series/ RTL8111H Series/ RTL8107E Series | External | X | X | X | X | O |
| RTL8111GS Series/ RTL8111GUS Series/ RTL8111HS Series/ RTL8106EUS Series/ RTL8107ES Series/ RTL8118AS Series | SWR | O | O | O | X | X |
| RTL8106E Series | LDO | X | X | X | X | X |

Note:

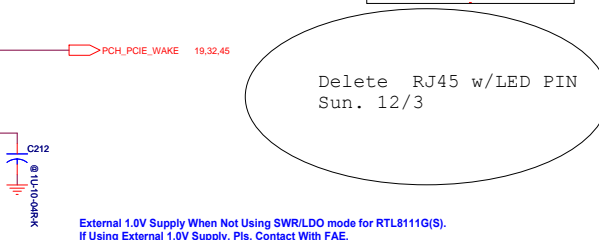
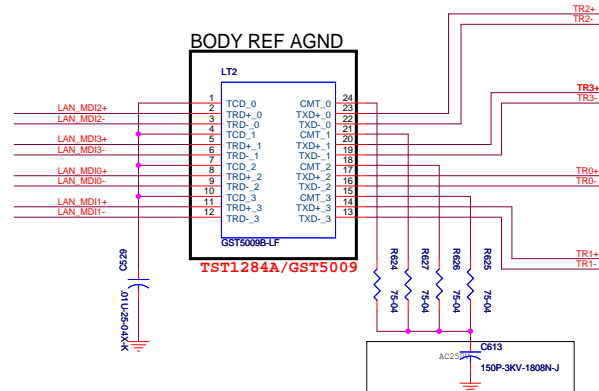
1. R1 is reserved for the convenience of changing the 1.0V supply source between SWR/LDO mode and external supply. No design change of PCB model is needed with R1 reserved.

If only one 1.0V supply source is selected for one PCB model, i.e. no other choices are reserved:

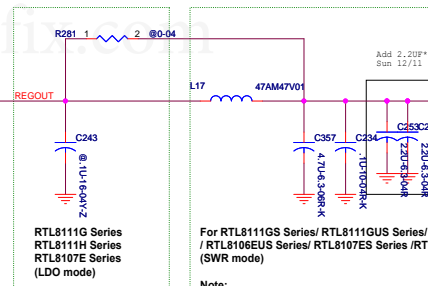
a. For RTL8111G Series, RTL8111H Series and RTL8107E Series, LDO mode only

b. For RTL8111G Series, RTL8111H Series and RTL8107E Series, External 1.0V supply source.

a. For RTL8111GS Series, RTL8111GUS Series, RTL8111HS Series, RTL8106E Series, RTL8106EUS Series, RTL8107ES Series and RTL8118AS Series, External 1.0V Supply is Not Permitted.



External 1.0V Supply When Not Using SWR/LDO mode for RTL8111G(S).
If Using External 1.0V Supply, Pls. Contact With FAE.



For RTL8111G Series/ RTL8111GUS Series/ RTL8111HS Series/ RTL8111G(S) Series/ RTL8111GUS Series/ RTL8111H(S) Series/ RTL8106EUS Series/ RTL8107E(S) Series/ RTL8118AS Series

Note:
Other than Lx, no inductor or bead should be placed on the path from REGOUT to VDD10.

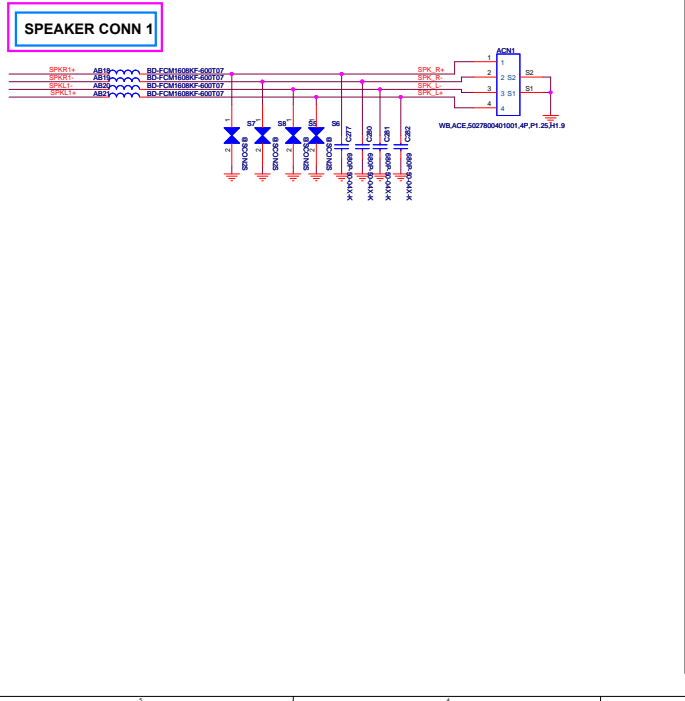
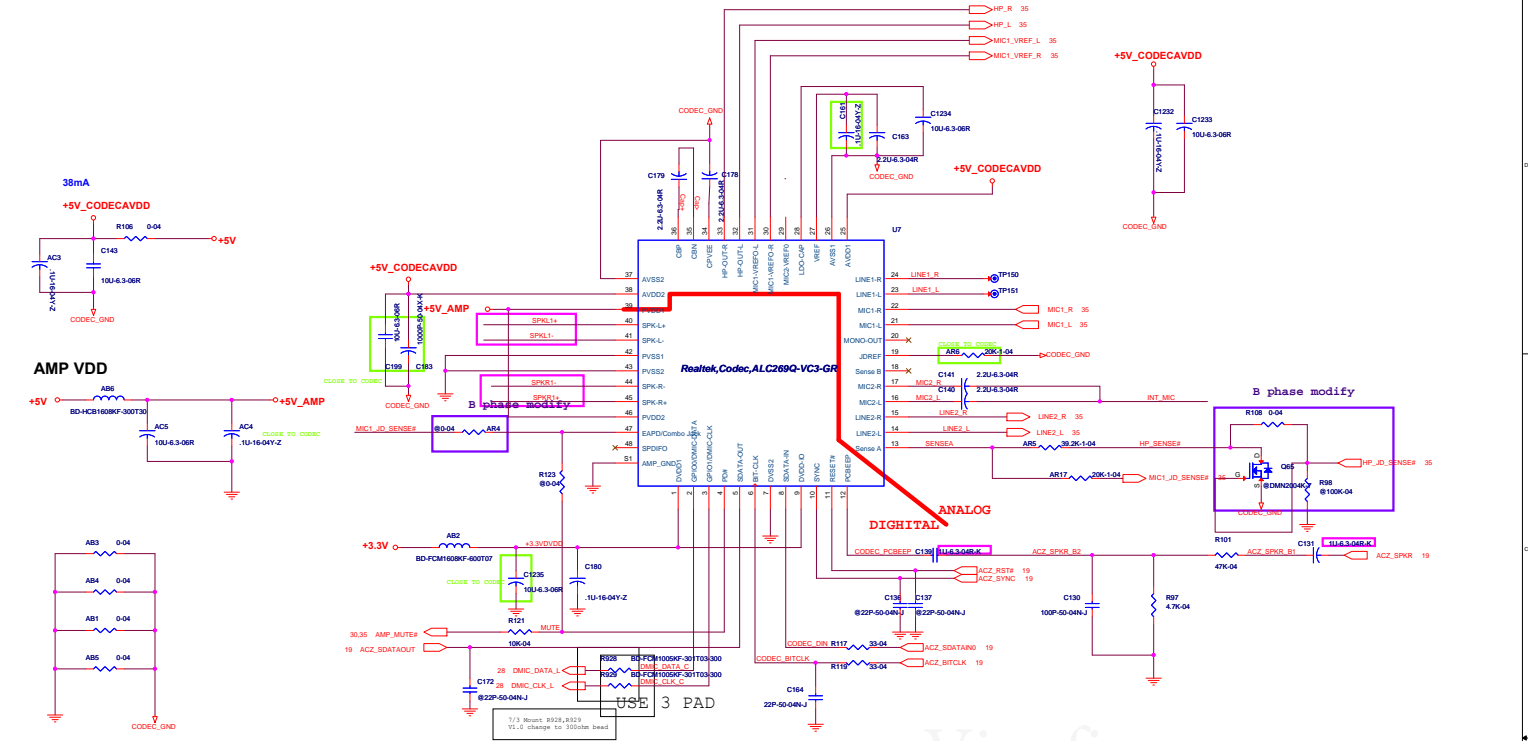
For RTL8111G(S)
* Place C3 to C6 close to each VDD10 pin-- 3, 8, 22, 30

For RTL8106E
* Place C3 to C4 close to each VDD10 pin-- 8, 30

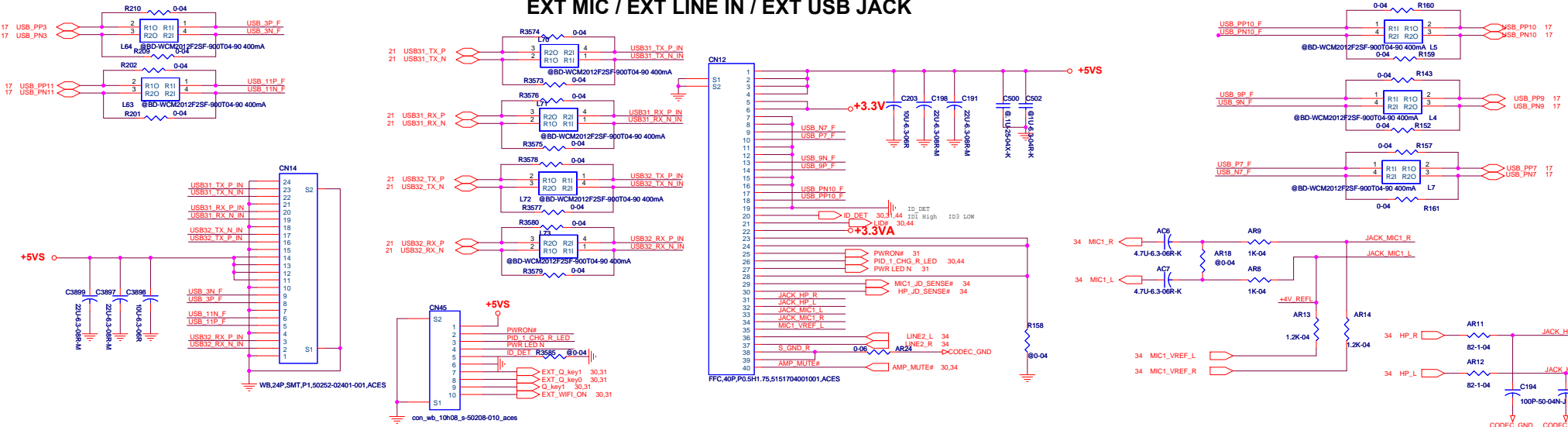
For RTL8106E
* Place C358 C250 close to each VDD10 pin-- 30 (reserve)

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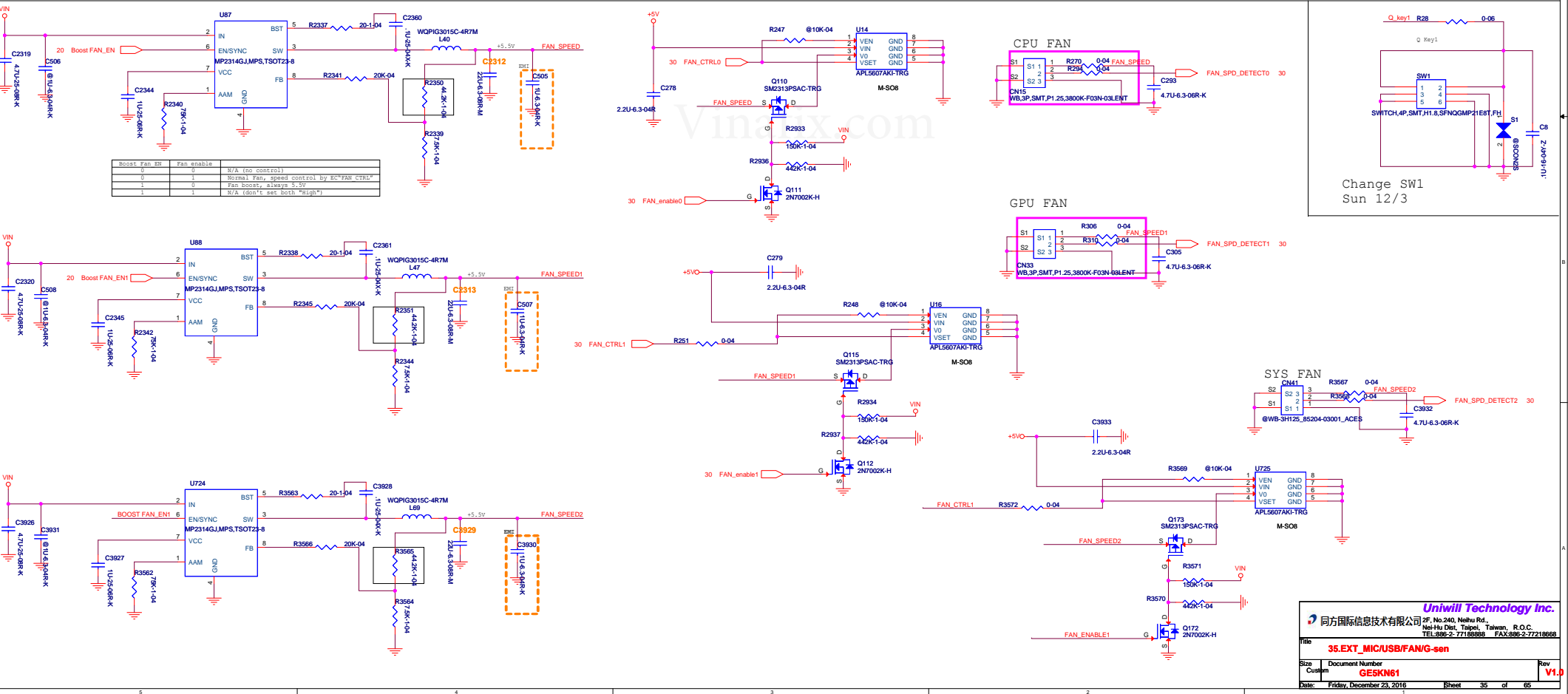
CODEC ALC269Q

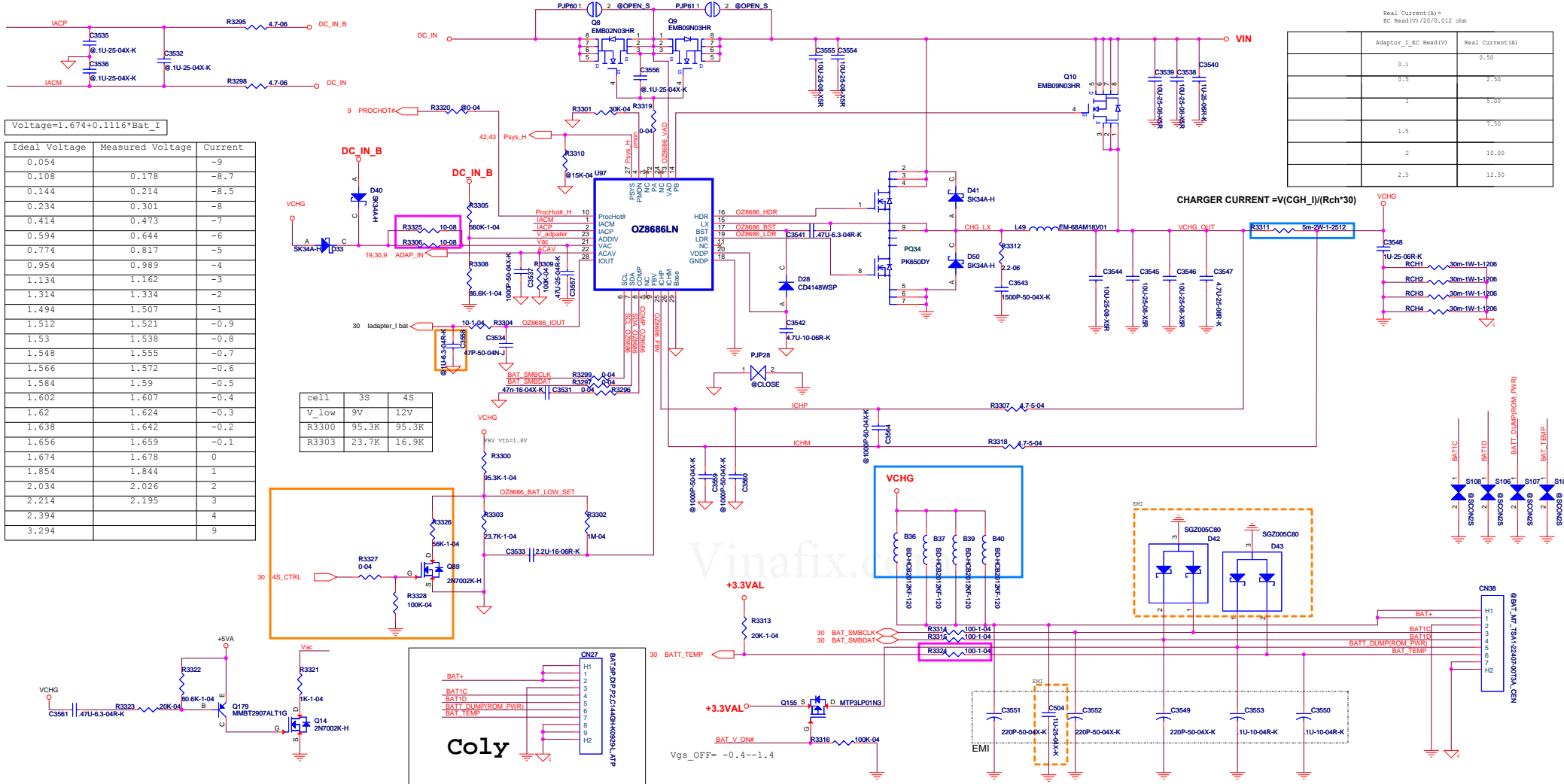


EXT MIC / EXT LINE IN / EXT USB JACK

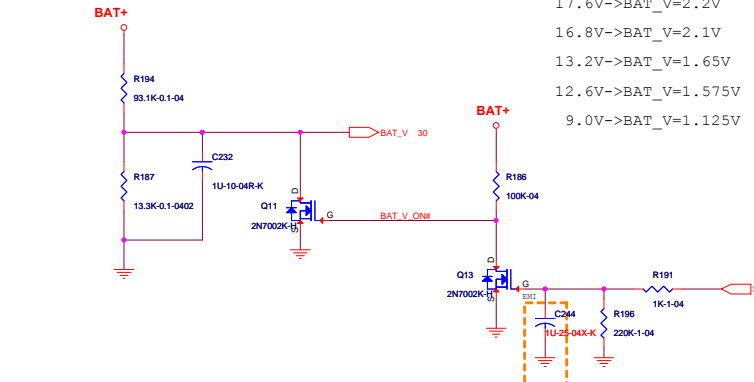


FAN CONTROLLER





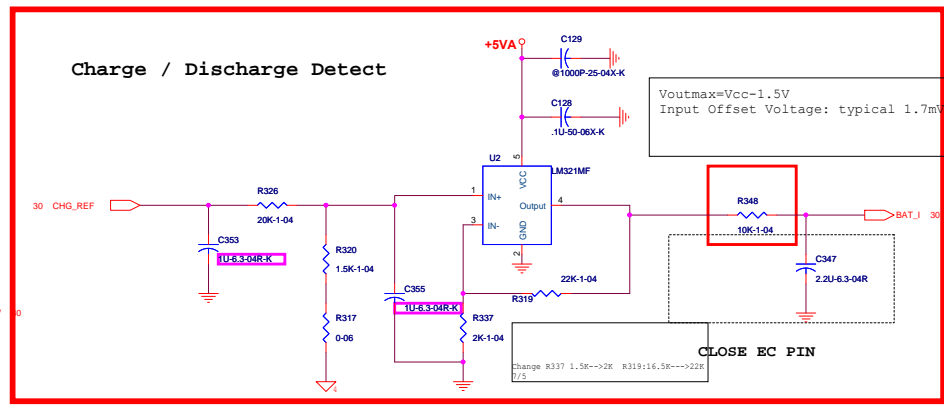
Battery Voltage Detect



17.6V->BAT_V=2.2V
 16.8V->BAT_V=2.1V
 13.2V->BAT_V=1.65V
 12.6V->BAT_V=1.575V
 9.0V->BAT_V=1.125V

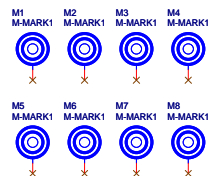
6/12

Charge / Discharge Detect



Voutmax=Vcc-1.5V
 Input Offset Voltage: typical 1.7mV max:7mV/9mV

CN42
DCIN_WO_2DC3003-002211_SIN



H13 H14 H15 H16 H18 H19 H20

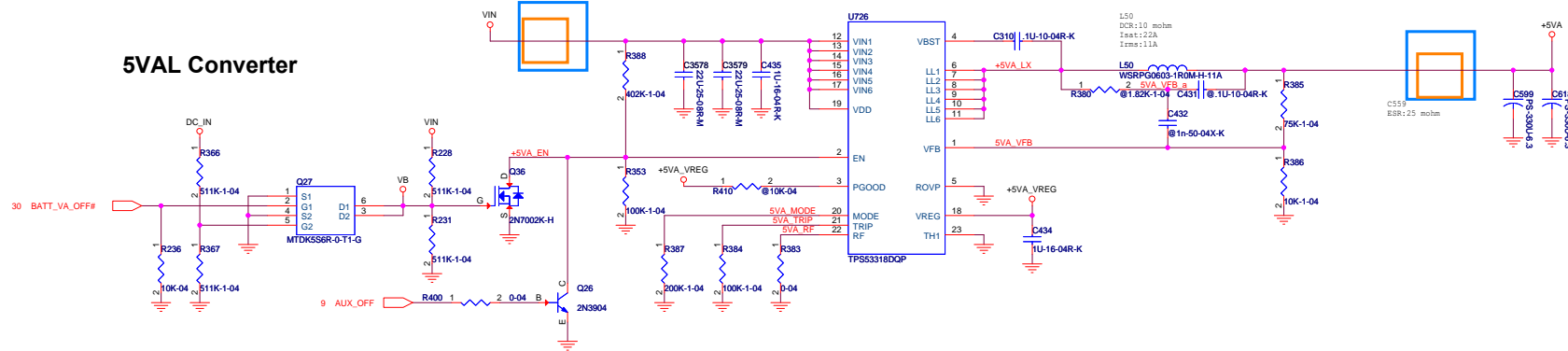
● SCHRZ12-1023-1C26
● SCHRZ12-1023-1C26
● SCHRZ12-1023-1C26
● SCHRZ12-1023-1C26
● SCHRZ12-1023-1C26
● SCHRZ12-1023-1C26
● SCHRZ12-1023-1C26

Pin connection diagram for the WB.HEF.08T-W-10A.10.SMT module. The module is represented as a 10-pin connector with pins labeled S1 through S10. Pin 1 (S1) is connected to a 3.3V supply. Pin 2 (S2) is connected to ground. Pins 3 through 10 are connected to a 3.3V supply. A table on the right lists the pin connections for the module:

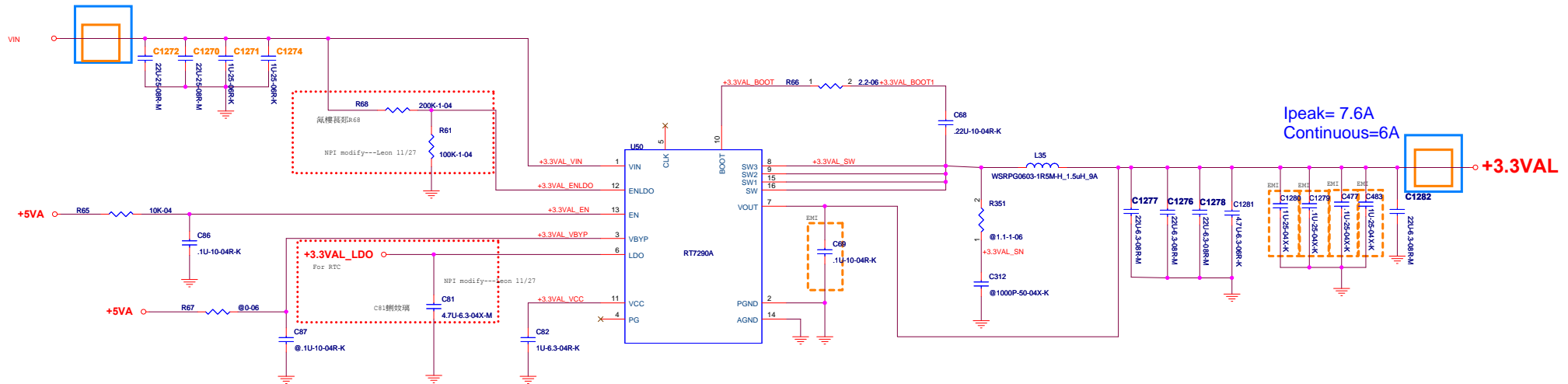
| Pin | Signal |
|-----|----------|
| 16 | PLT_RST# |
| 21 | CLK_TPM |
| 21 | LPC_AD0 |
| 21 | LPC_AD1 |
| 21 | LPC_AD2 |
| 21 | LPC_AD3 |
| 21 | LPC_AD4 |

WB-6H80_88460-0601_ACES

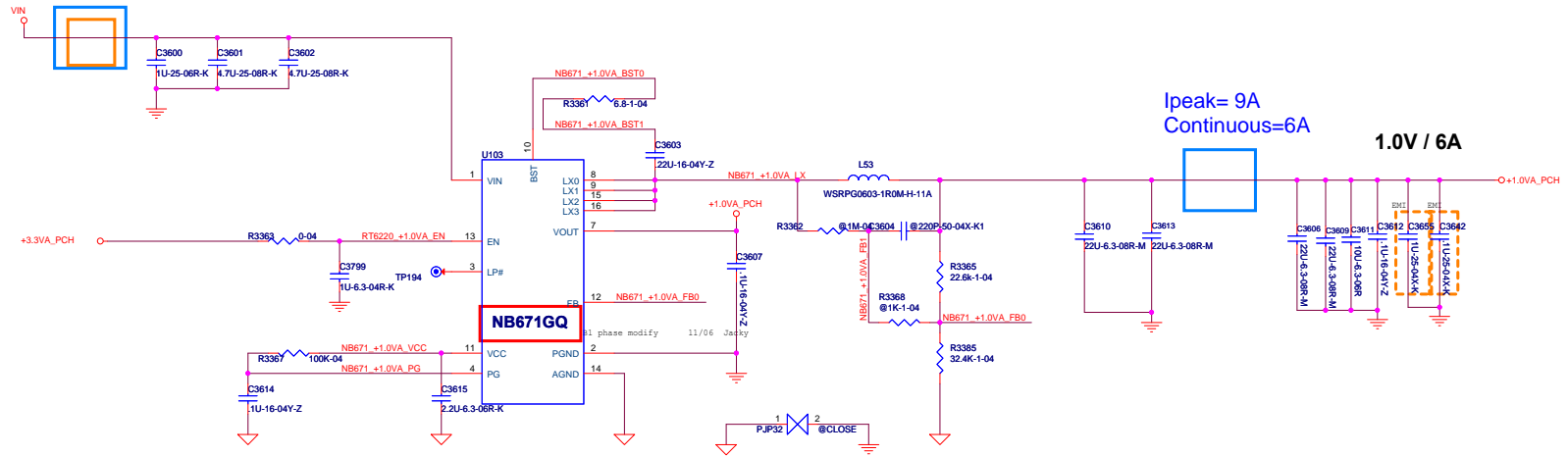
5VAL Converter



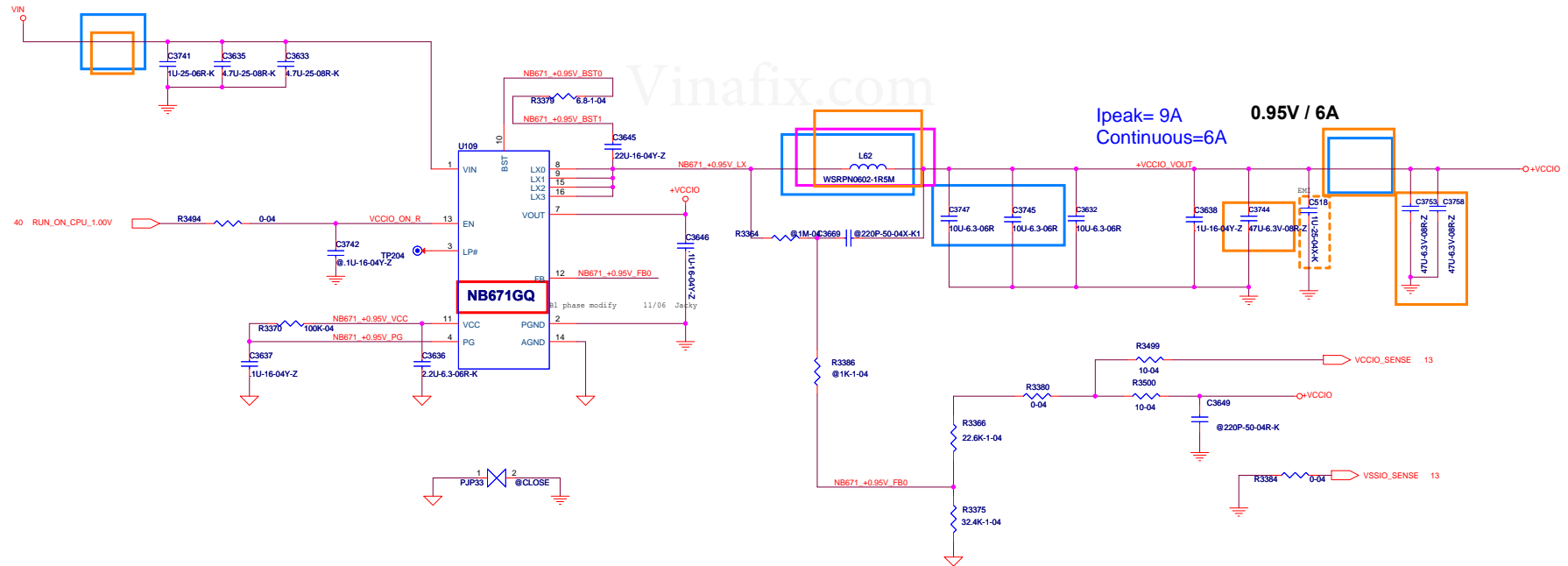
3.3VAL Converter



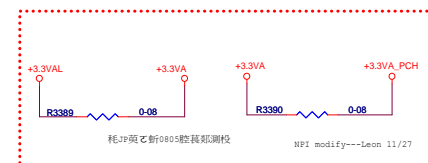
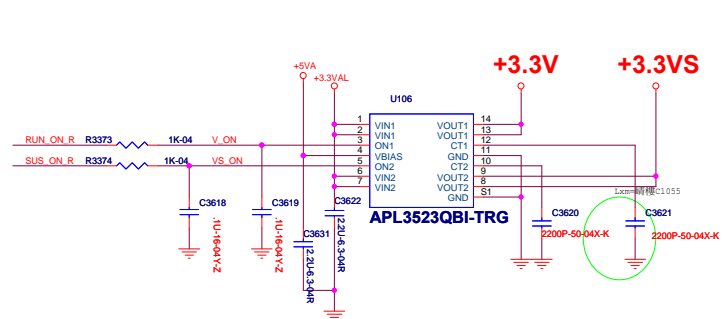
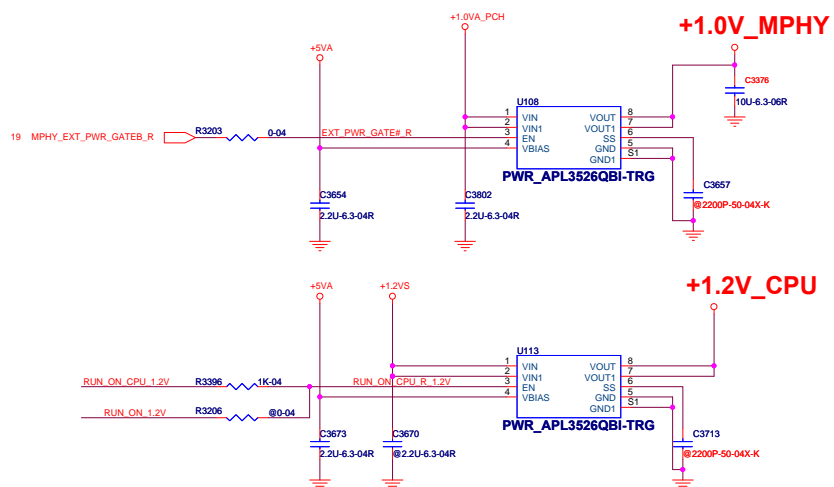
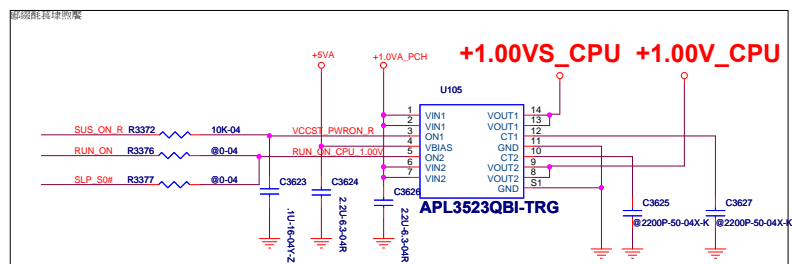
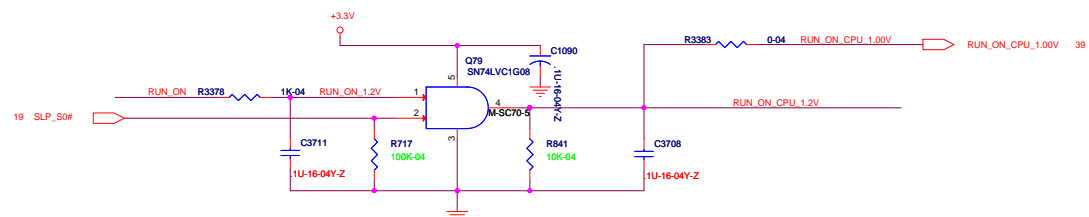
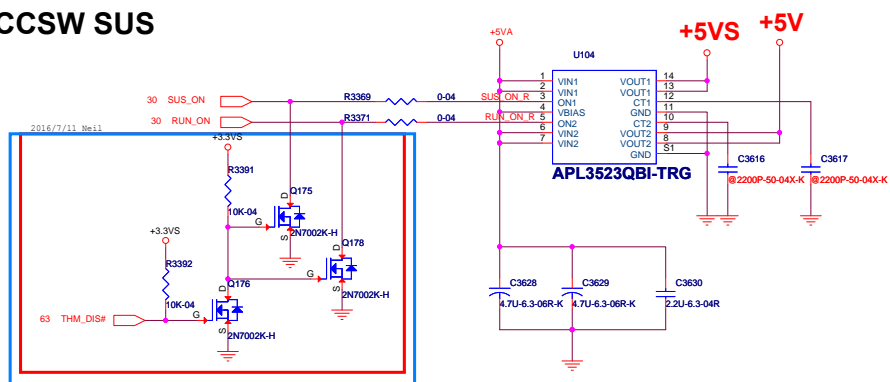
1.0VA Converter



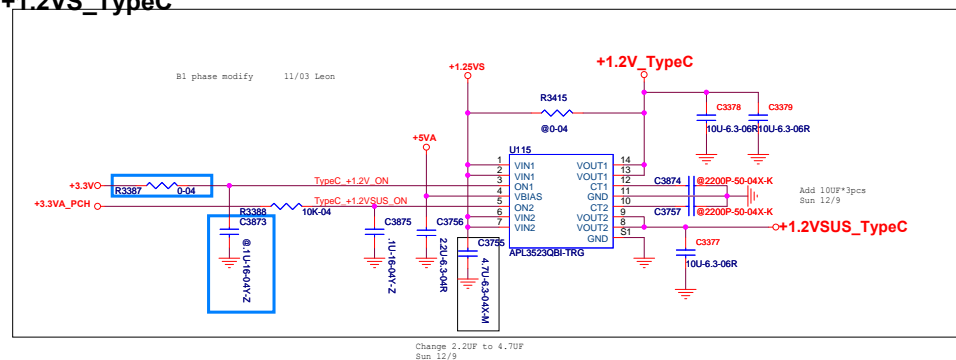
VCCIO Converter



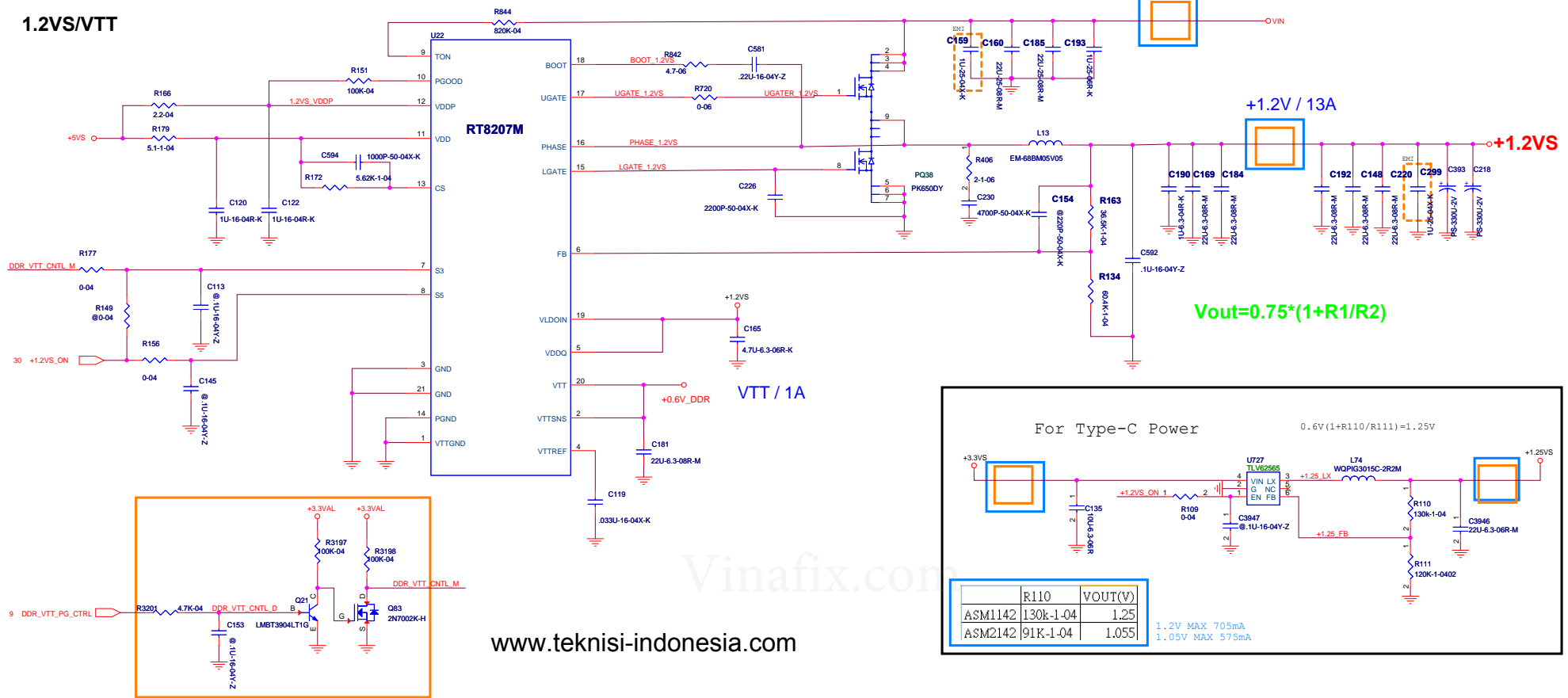
VCCSW SUS



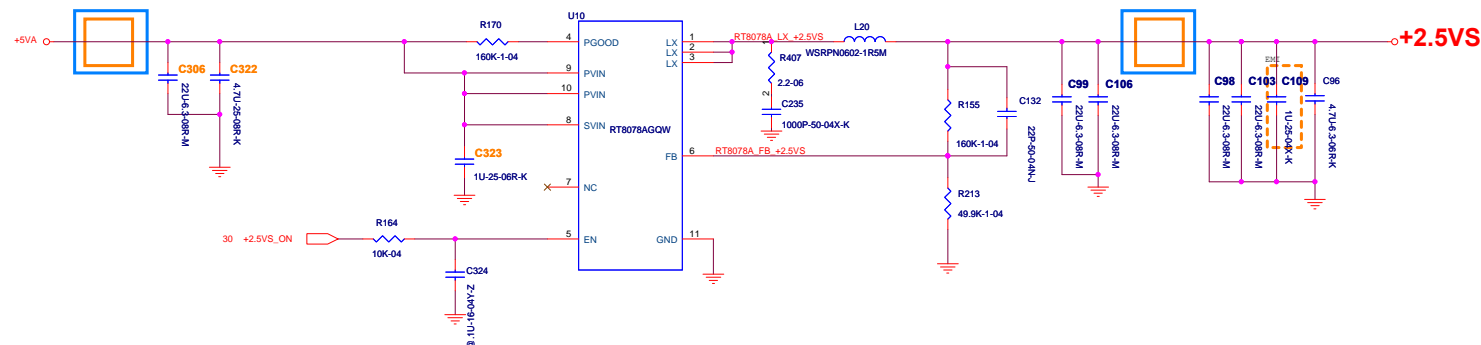
+1.2V_TypeC
+1.2VS_TypeC



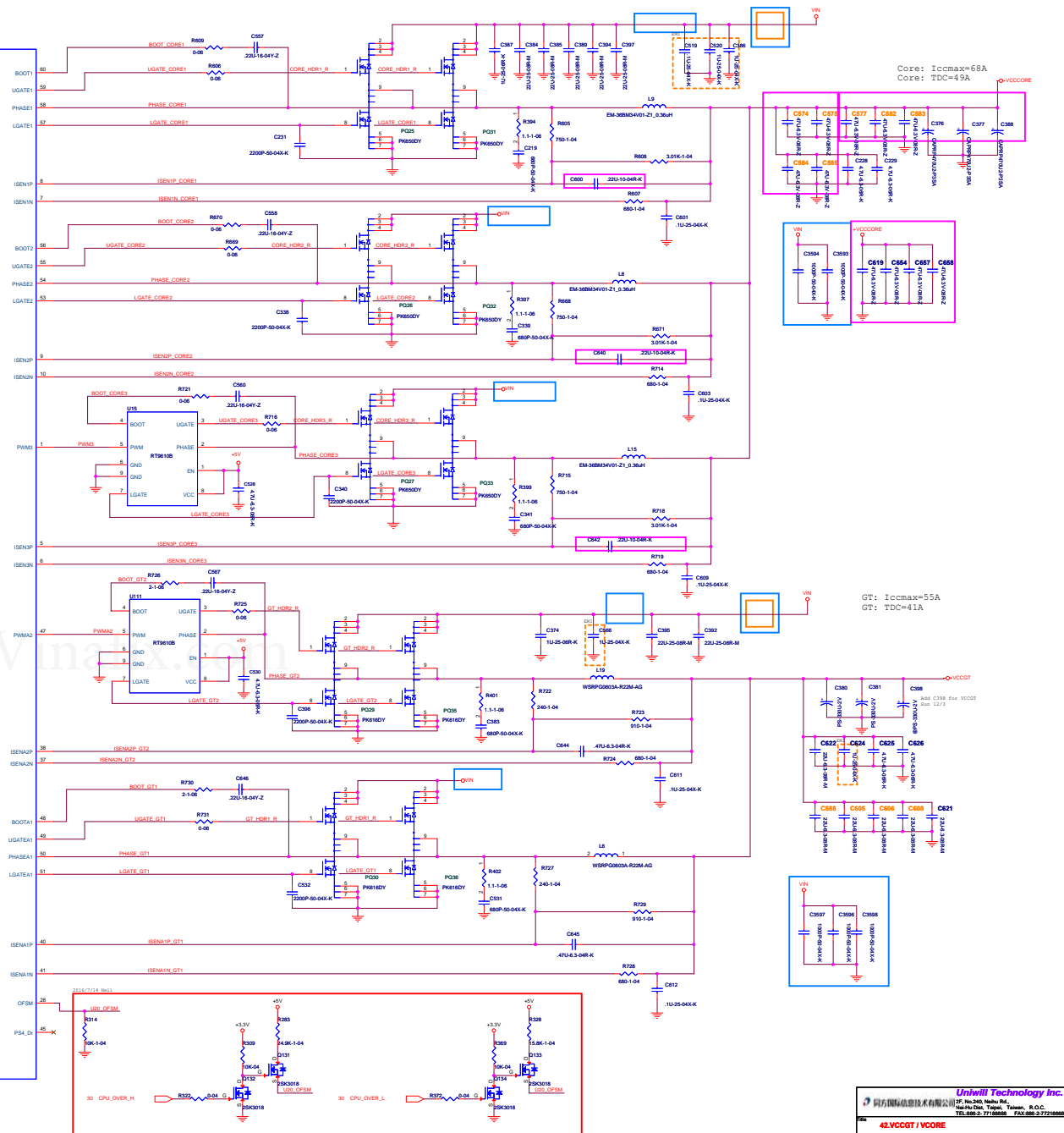
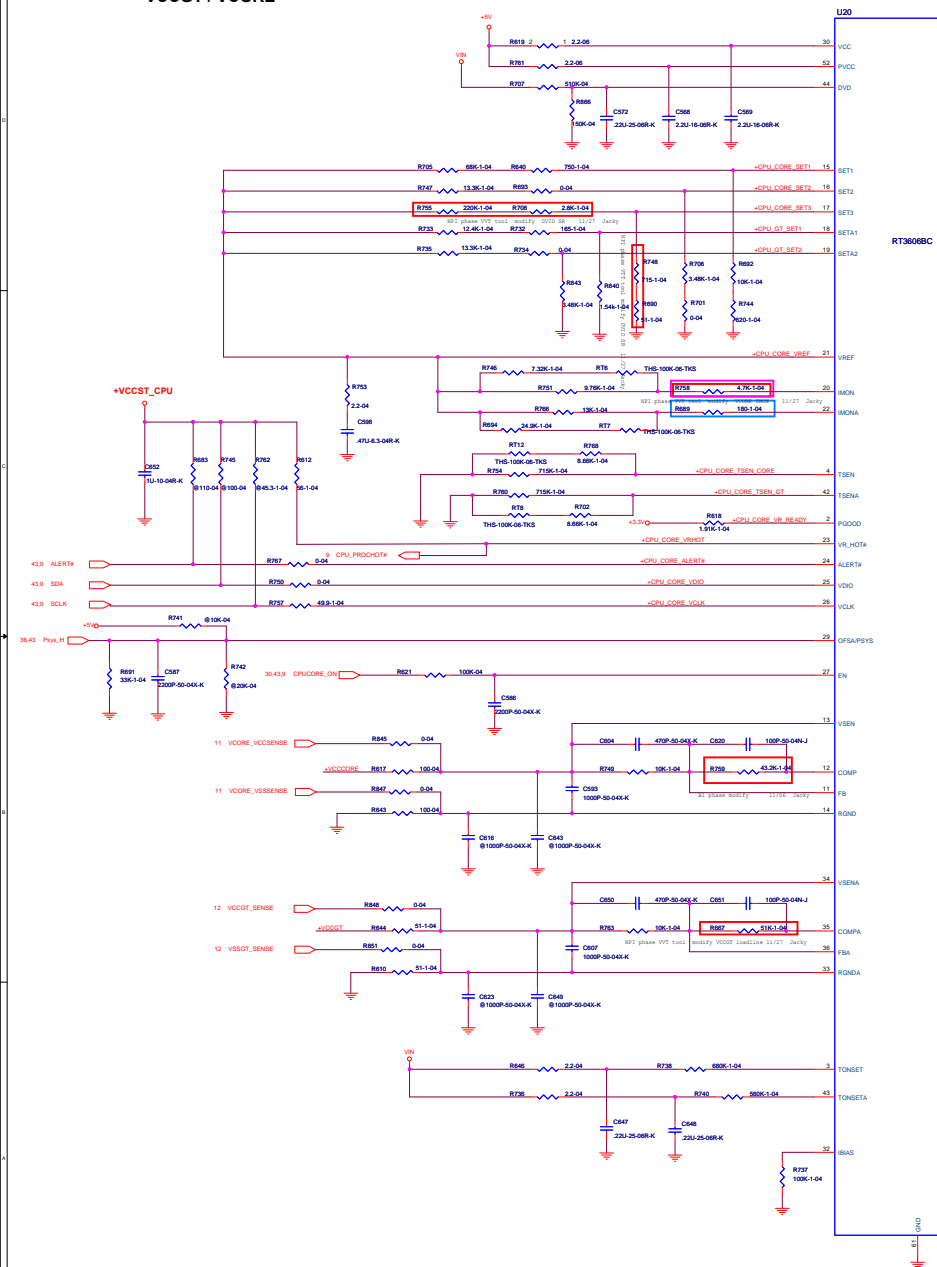
1.2VS/VT



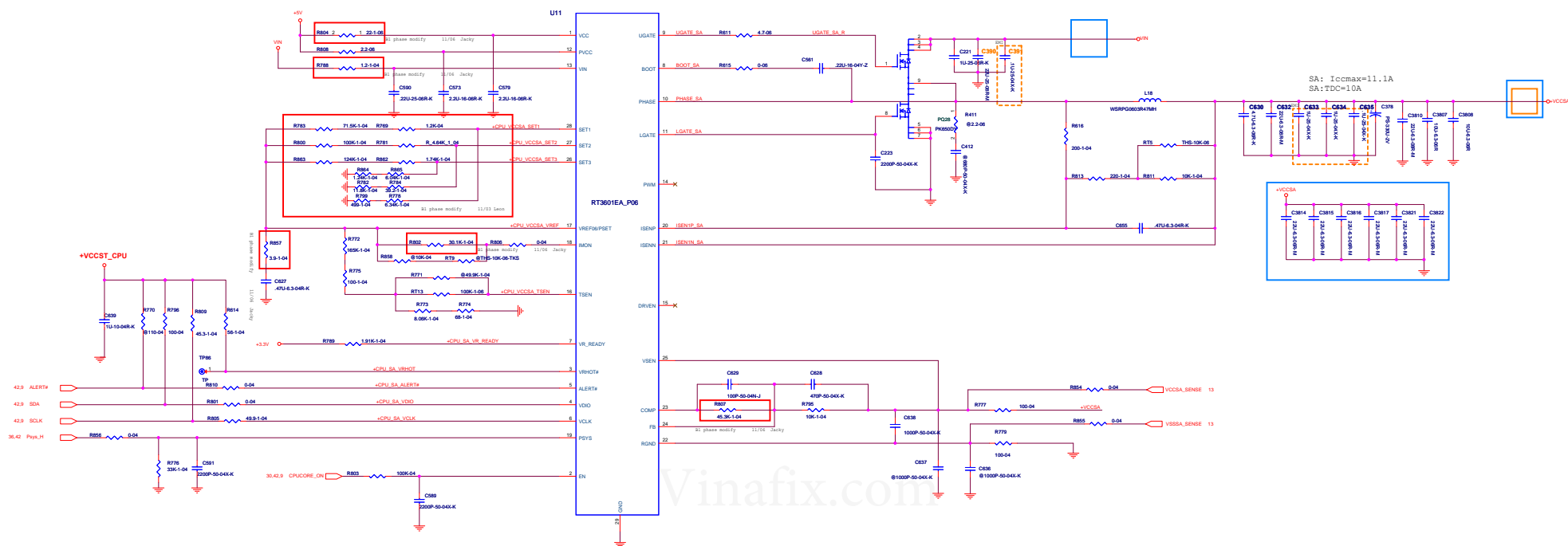
2.5VS Converter



VCCGT / VCORE

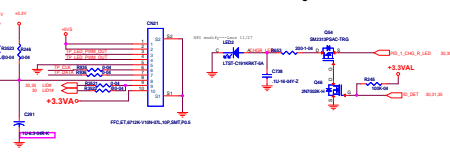


VCCSA

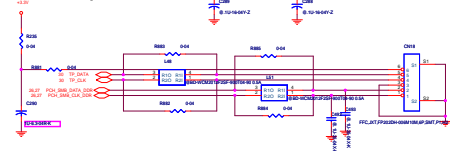


colay normal TP LED

Charge LED

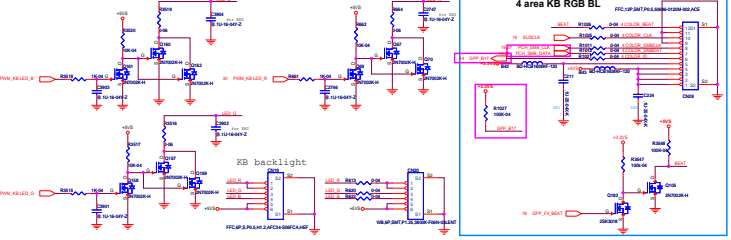
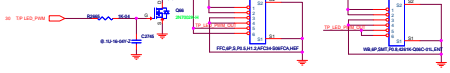


Click-pad

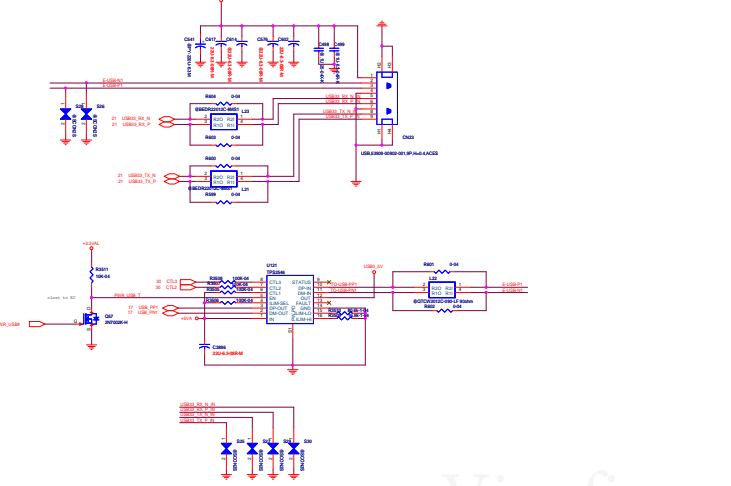


| | Power icon LED | KB | Pulse (TP) LED | Charging LED |
|------------------------------|----------------|-----|----------------|--------------|
| Power on | on | on | on | I |
| Fan 风扇 (Q-Key) | on | on | 蜂鸣器 | |
| Power off | off | off | off | |
| Suspend | 蜂鸣器(allow KB) | 蜂鸣器 | 蜂鸣器(allow KB) | |
| Charging | | | | on |
| Stop Charging (Full Battery) | | | | off |
| Power on/Battery Low (<60%) | | | | 闪烁 1.5s |

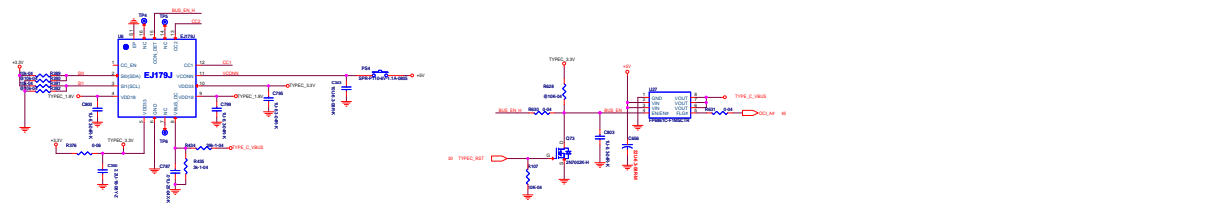
LED CONN



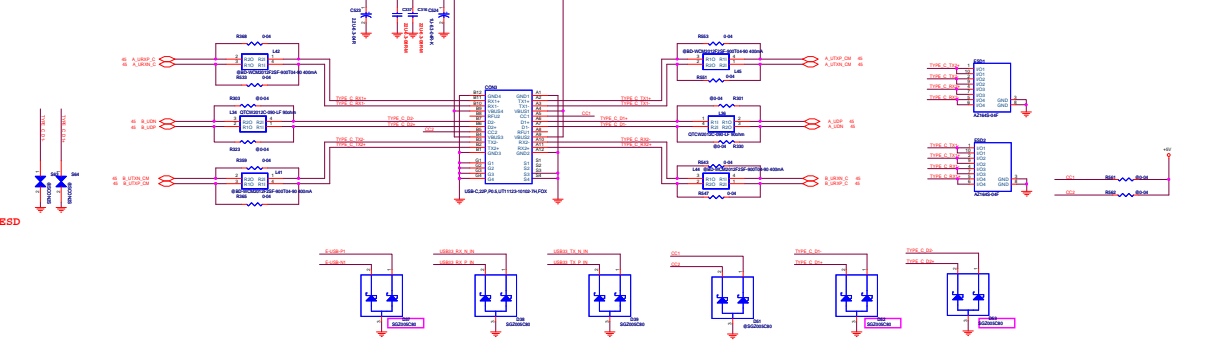
Type A USB3.0



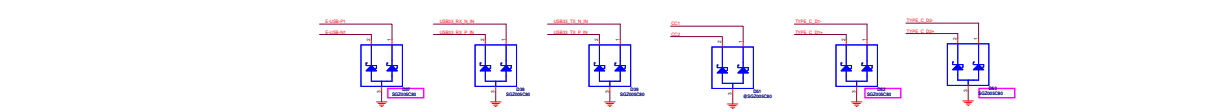
USB Type-C SWITCH

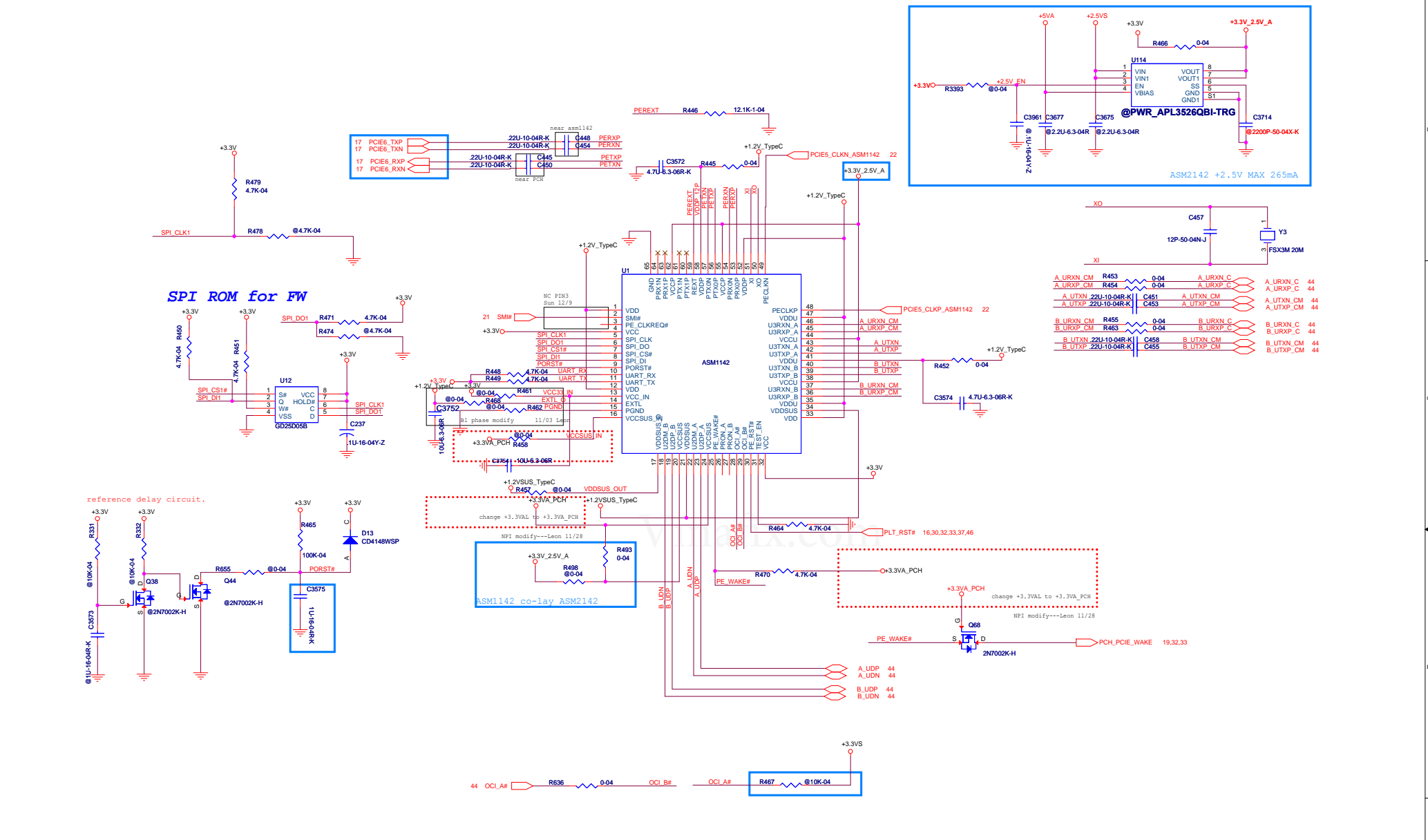


USB Type-C Port



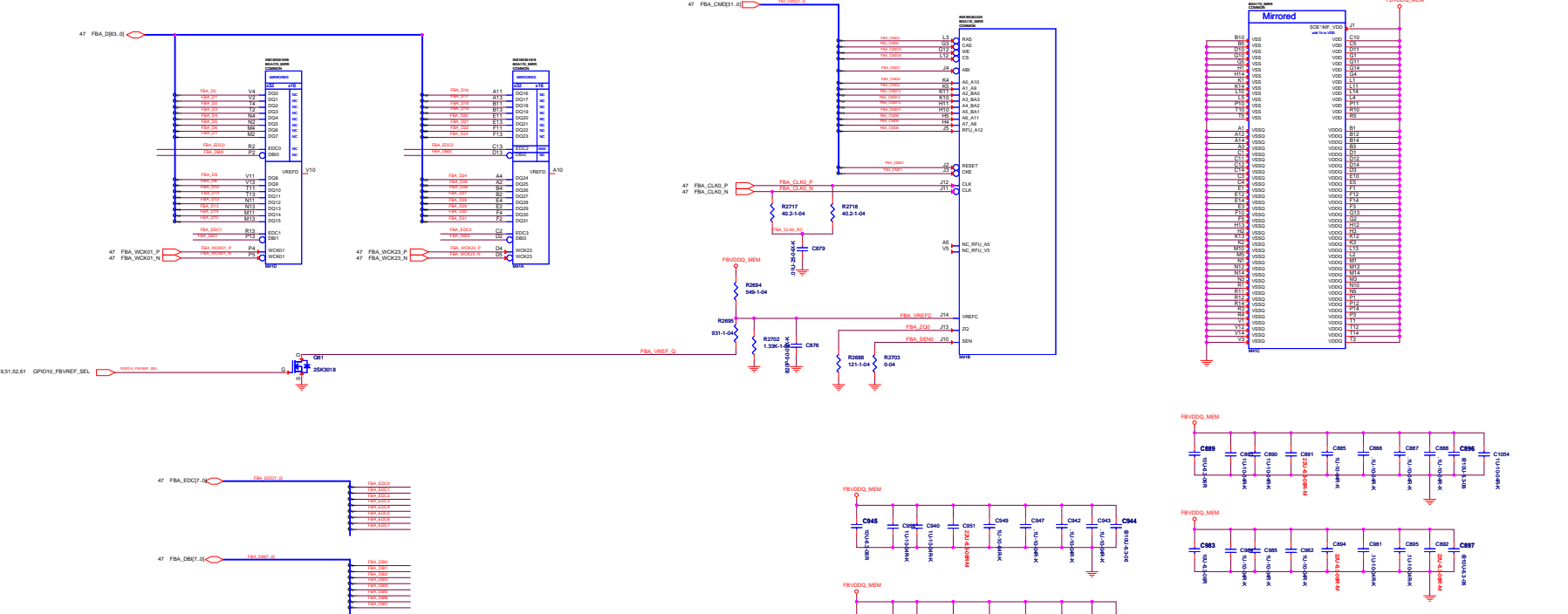
ESD



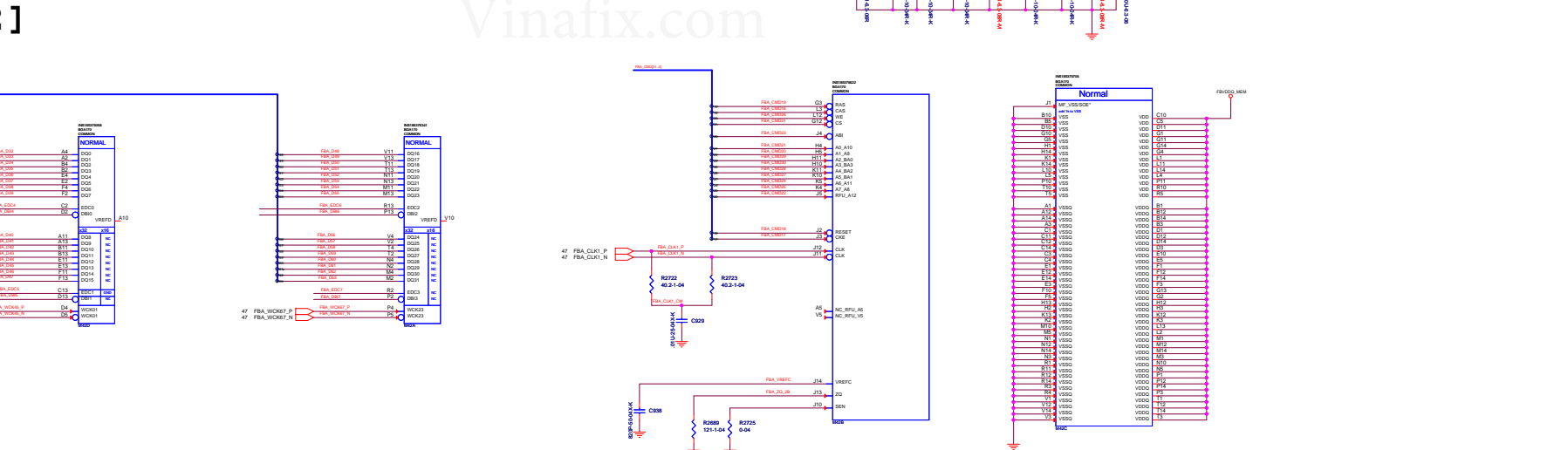


| 1142 | | | | 2142 | | | |
|--------|--------------------|------------|-----------|------|--|--|-----------|
| | | Pin | | | | | |
| VDD | Core power | 1, 12, 33 | 1.2V | | | | 1.05V |
| VCC | I/O power | 4, 32 | 3.3V | | | | 3.3V |
| VCCSUS | Suspend I/O power | 20 | 3.3V(SUS) | | | | 2.5V |
| VDDSUS | Suspend core power | 24 | 3.3V(SUS) | | | | 3.3V(SUS) |
| VDDU | USB | 35, 41, 47 | 1.2V | | | | 1.05V |
| VCCU | USB | 38, 44 | 3.3V | | | | 2.5V |
| VDDP | PCIE | 52, 58 | 1.2V | | | | 1.05V |
| VCCP | PCIE | 55, 62 | 3.3V | | | | 2.5V |

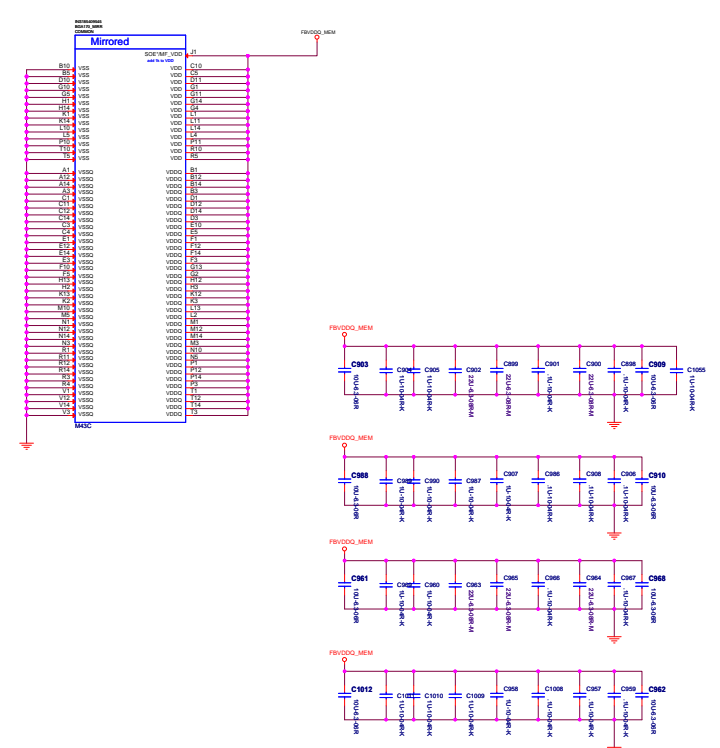
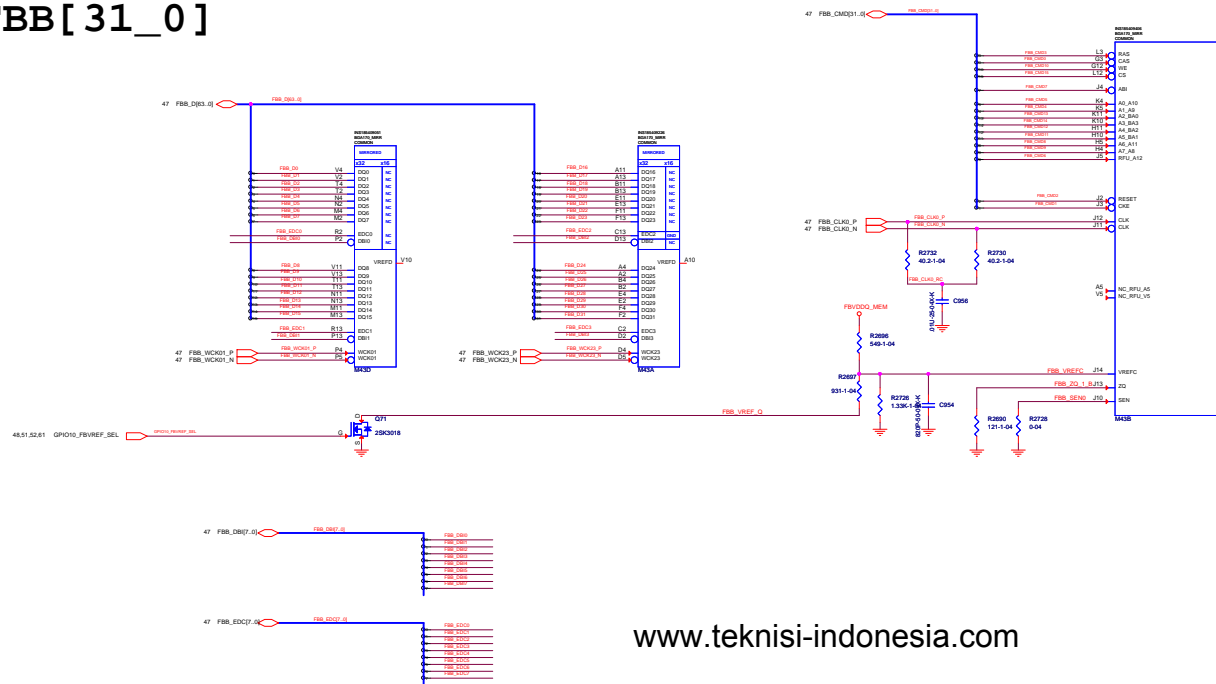
MEM_FBA[31_0]



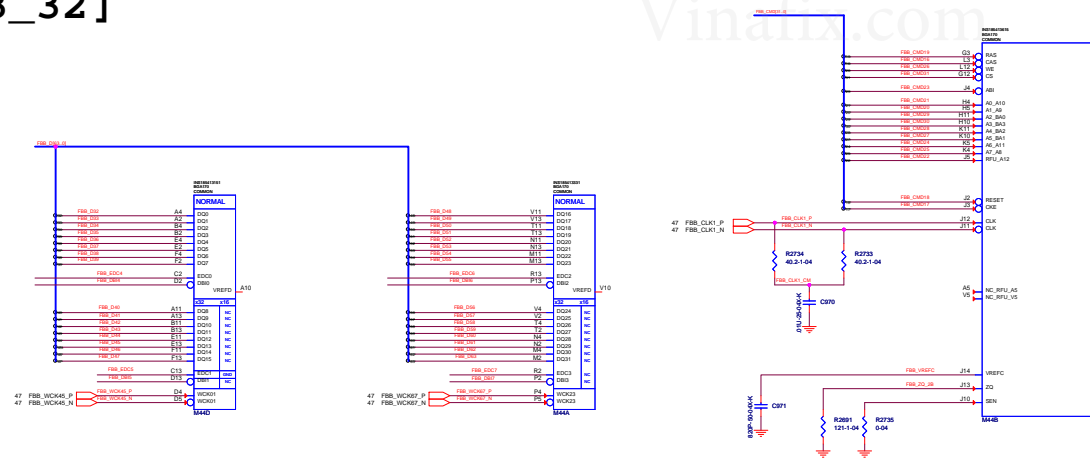
MEM_FBA[63_32]



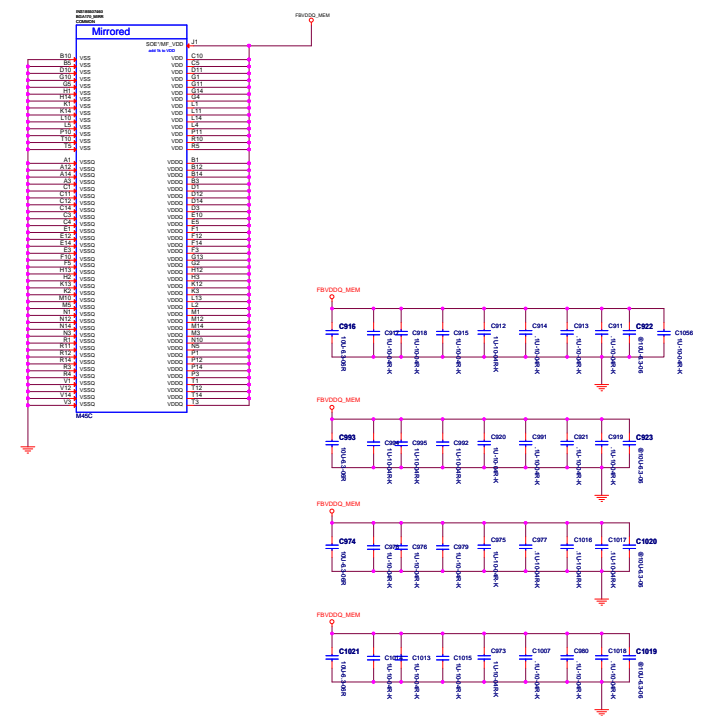
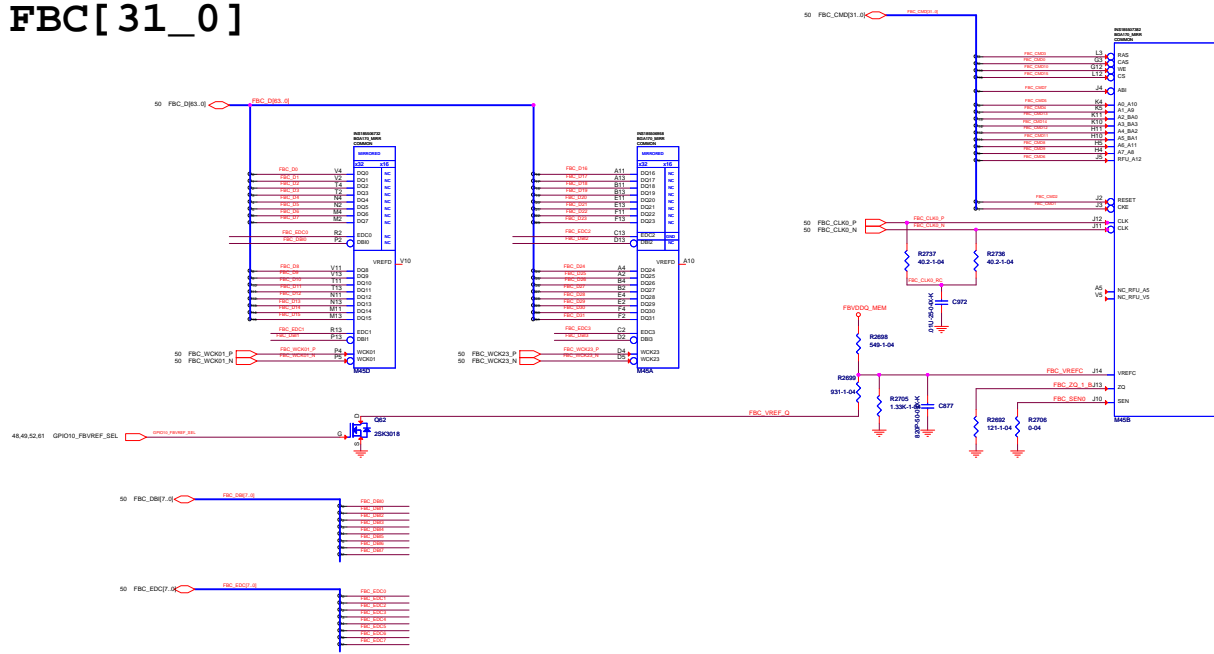
MEM_ FBB[31_0]



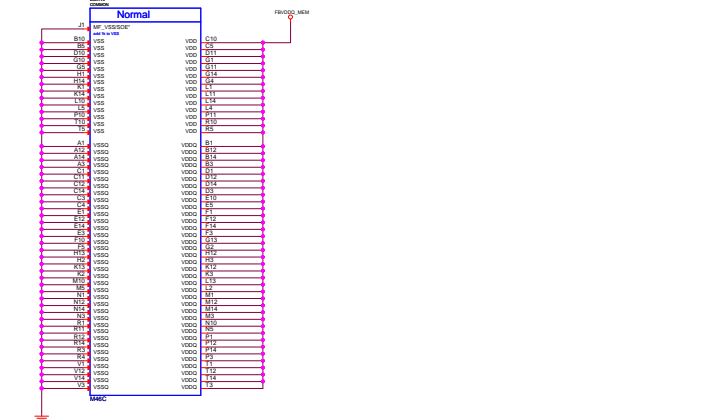
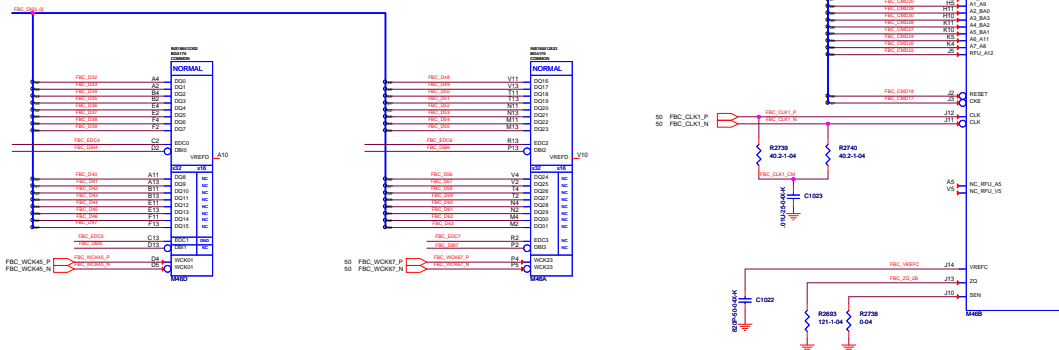
MEM_ FBB[63_32]



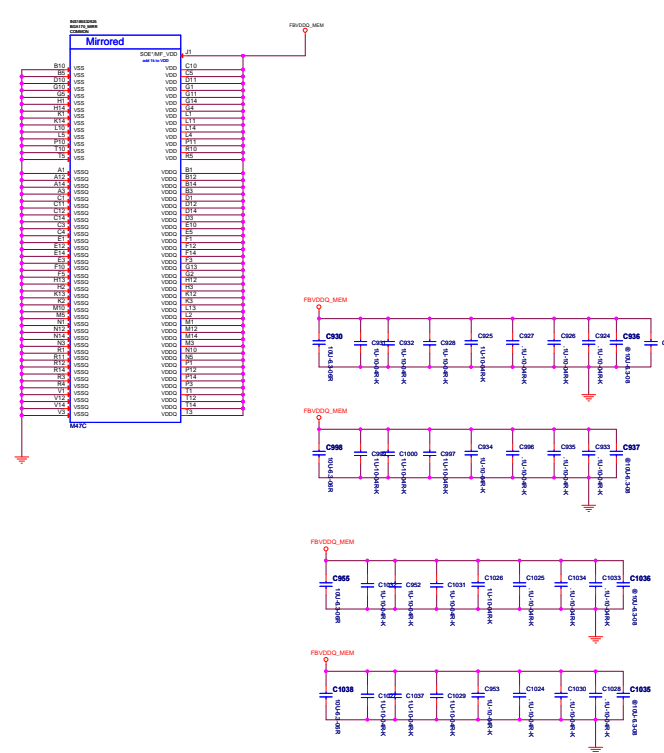
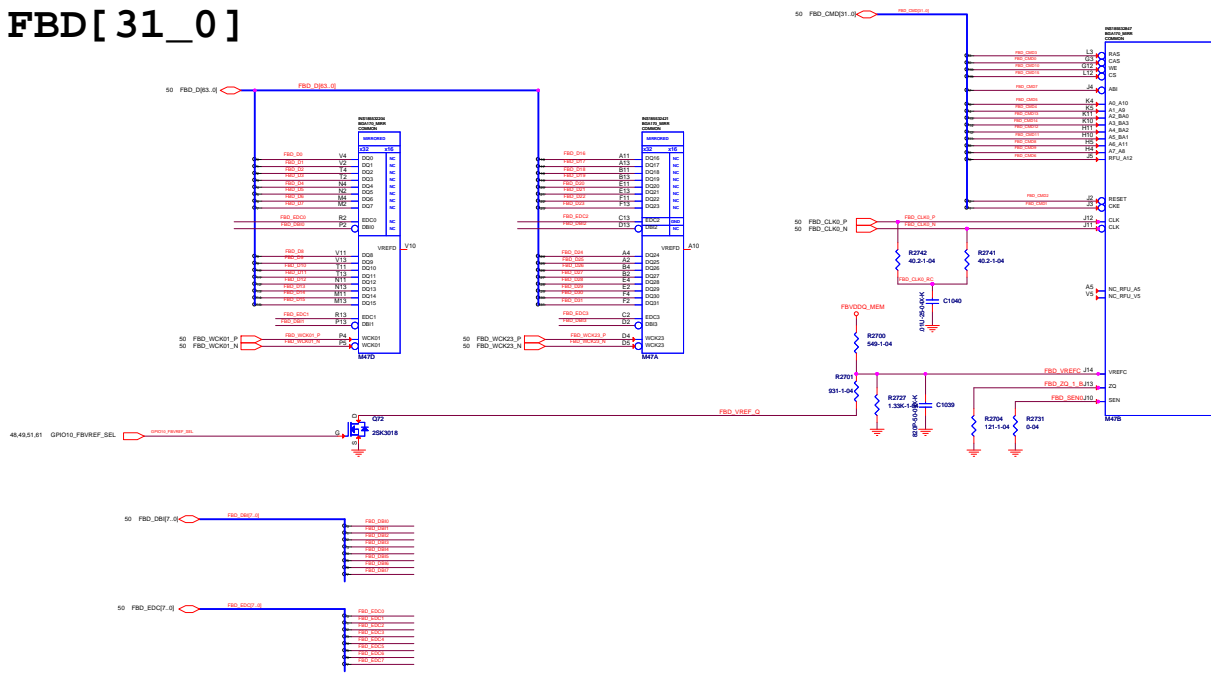
MEM_FBC[31_0]



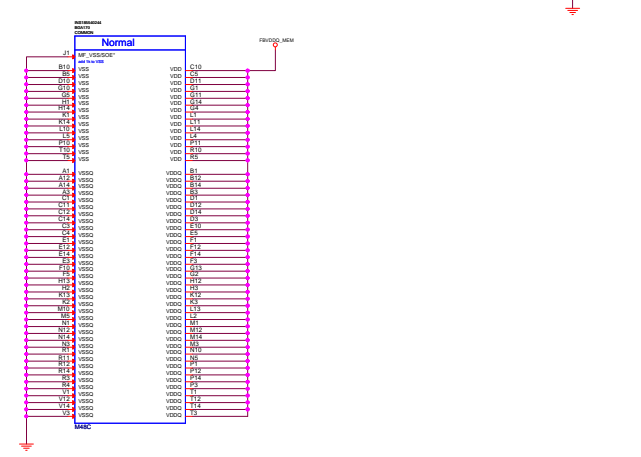
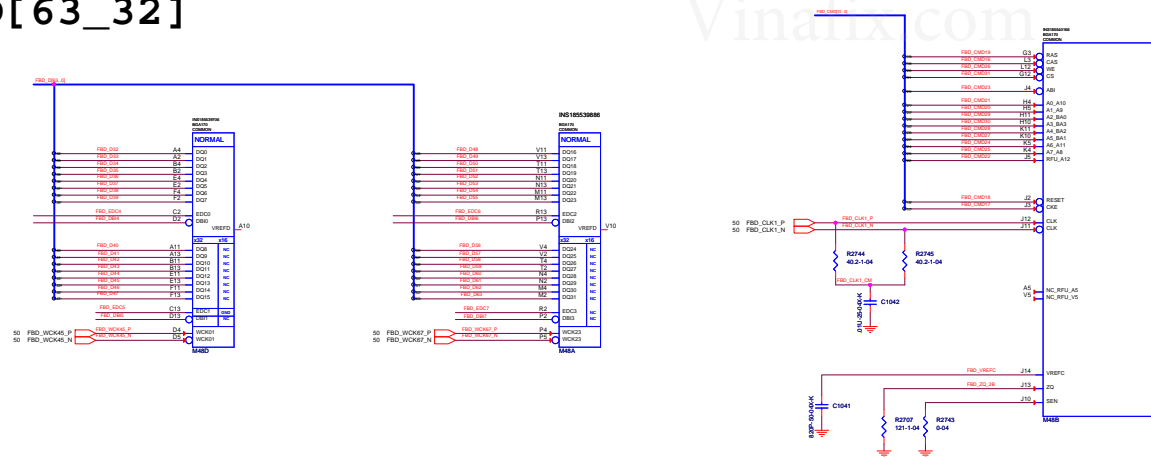
MEM_FBC[63_32]

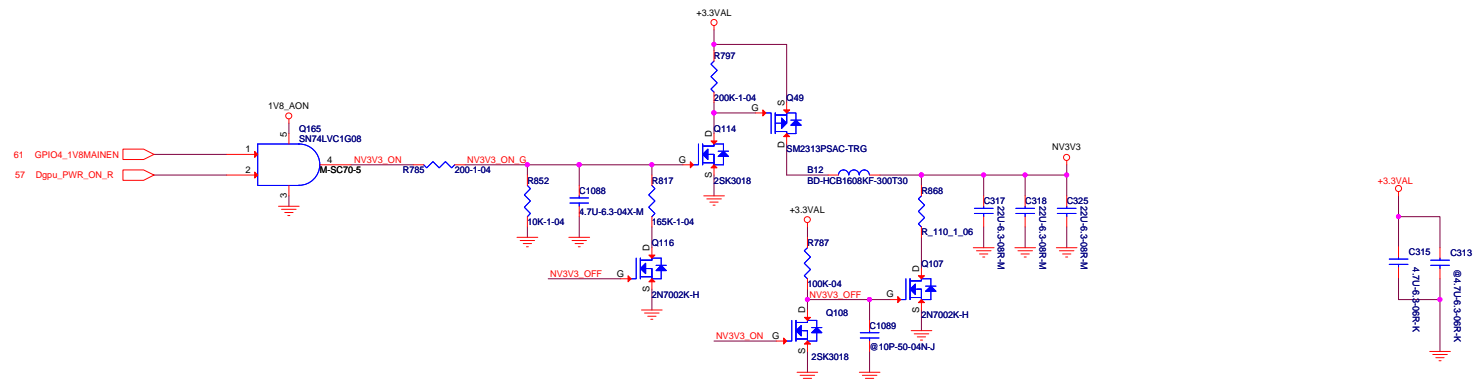


MEM_ FBD[31_0]

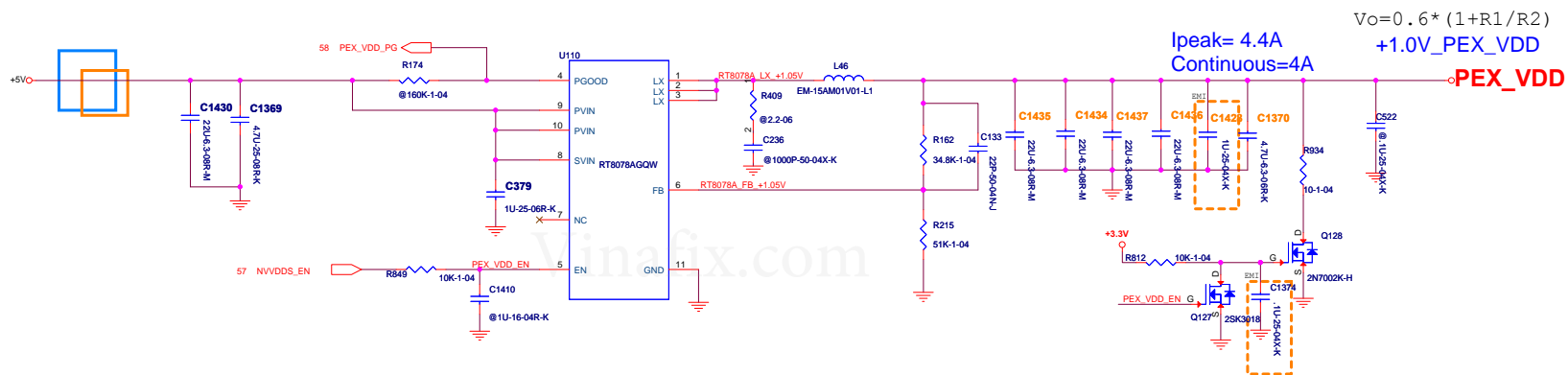


MEM_ FBD[63_32]

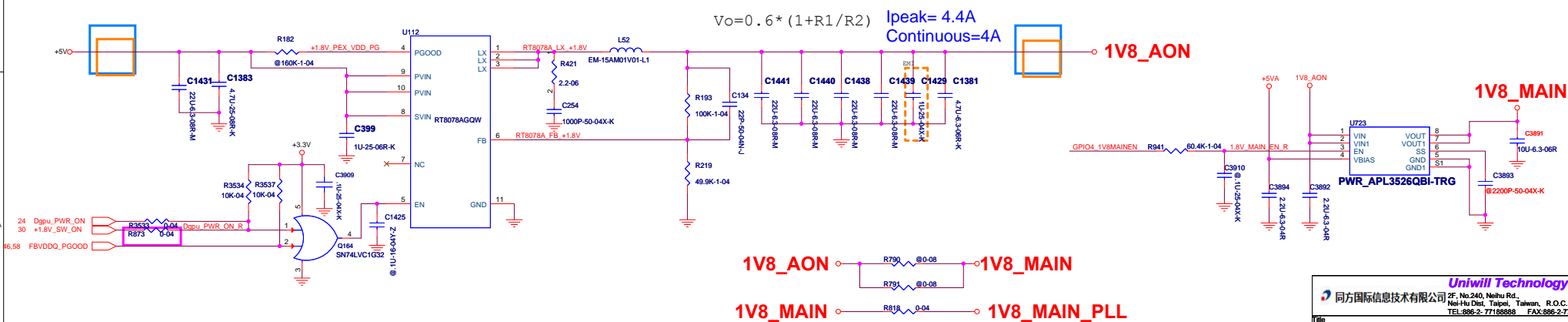


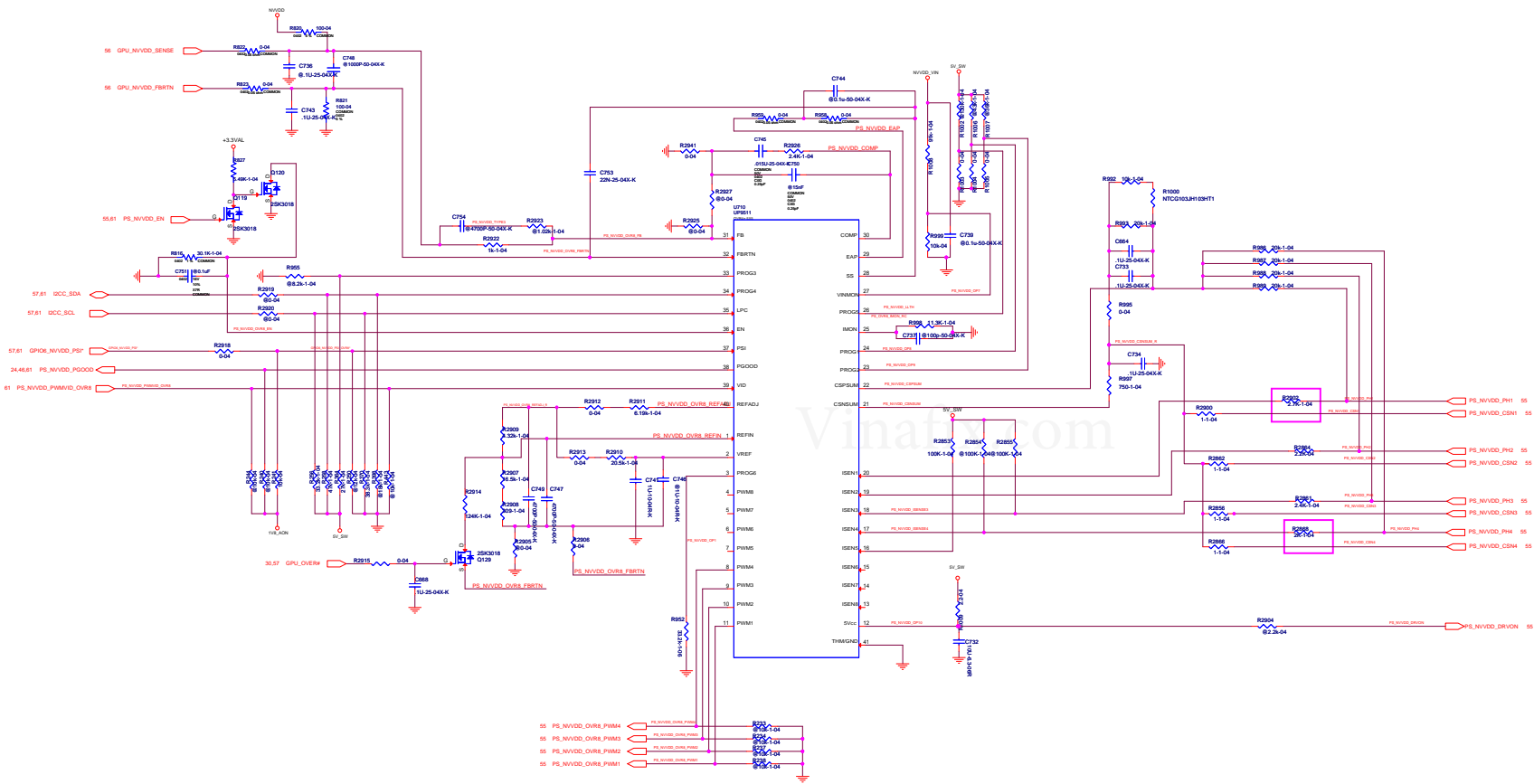


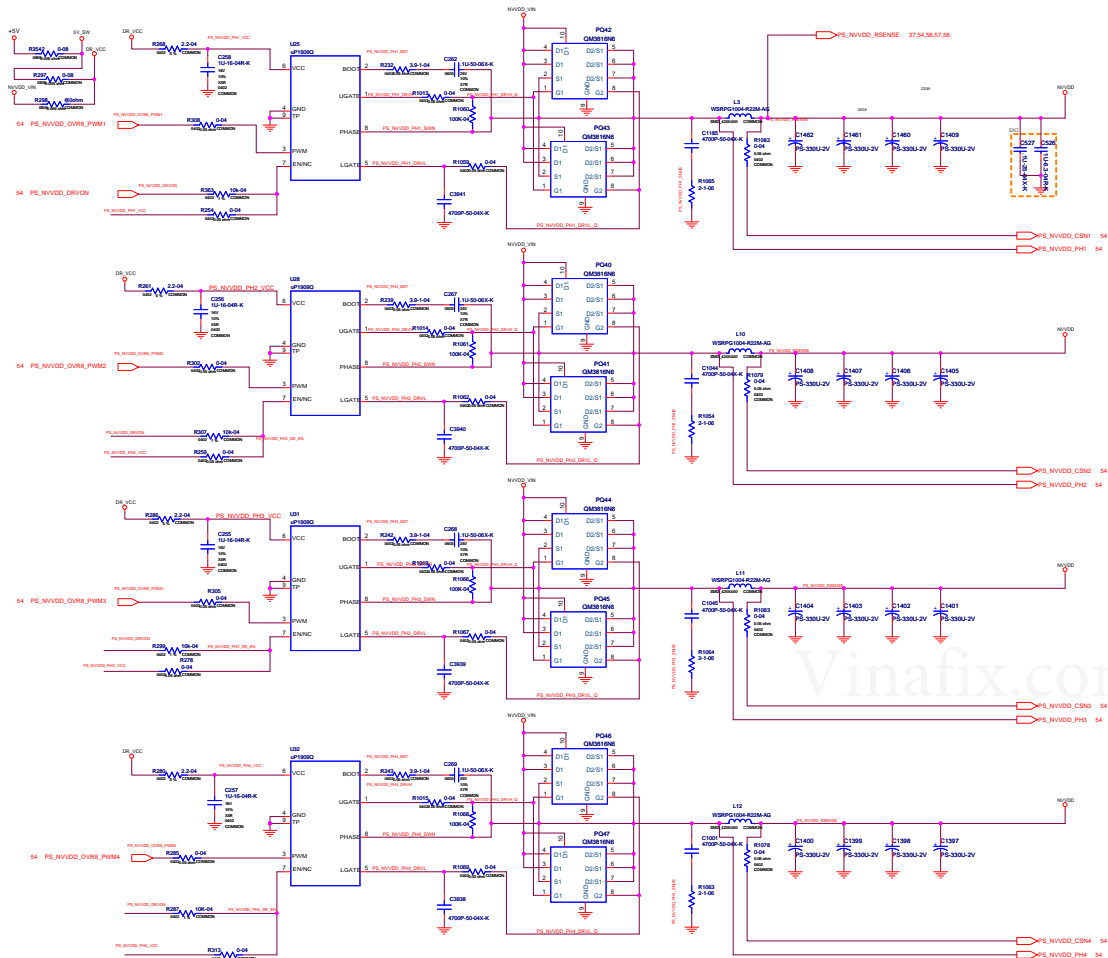
PEX_VDD Converter



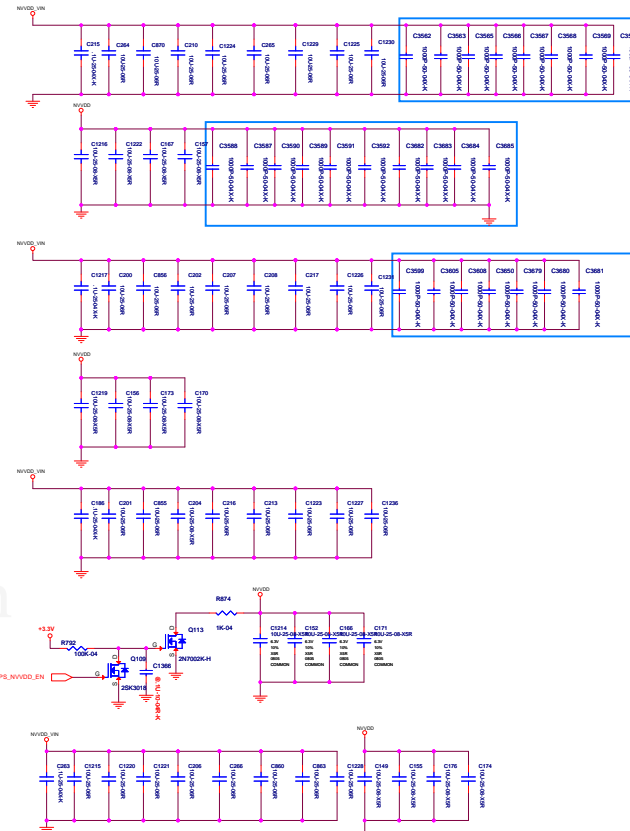
1.8V Converter





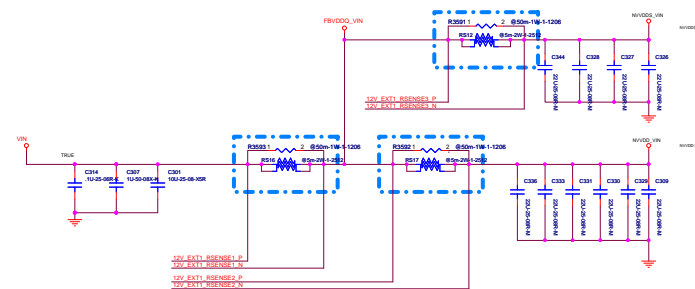


NVDD 0.5V-1.25V
 G2 ICC= 80/204 A
 G1 ICC= 62/164 A





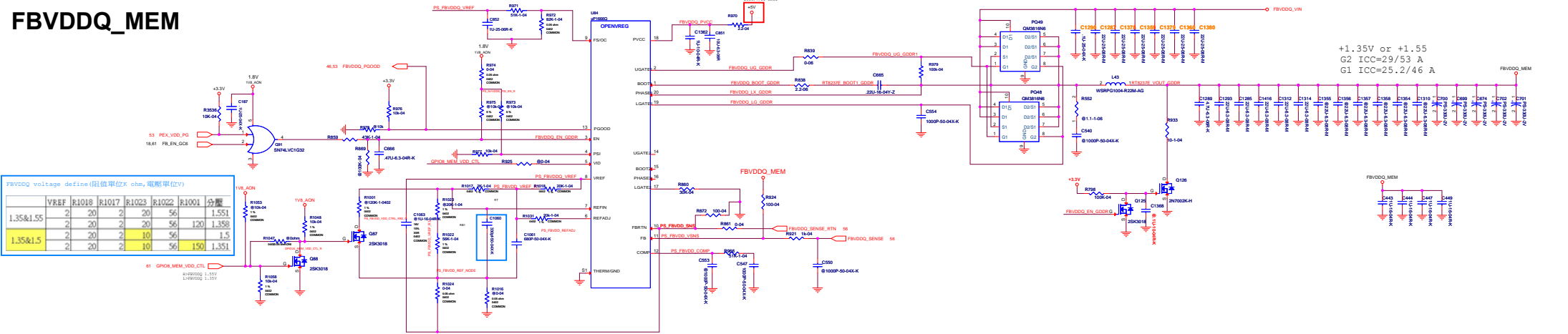
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FBVDDQ_MEM

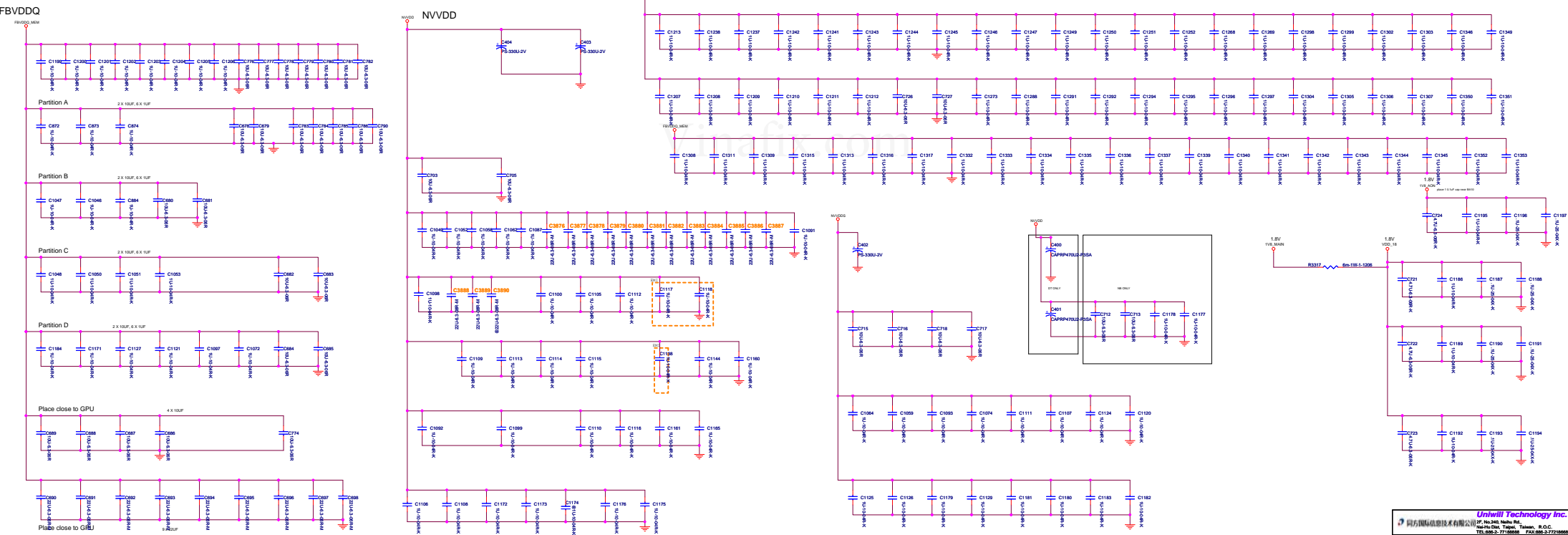
FBVDDQ voltage define (阻值單位K ohm, 電壓單位V)


| | VREF | R1018 | R1017 | R1023 | R1022 | R1001 | 分壓 |
|-----------|------|-------|-------|-------|-------|-------|----|
| 1.35&1.55 | 2 | 20 | 2 | 20 | 56 | 1.551 | |
| 1.35&1.5 | 2 | 20 | 2 | 10 | 56 | 1.5 | |



+1.35V or +1.55
G2 ICC=29/53 A
G1 ICC=25.2/46 A

Decoupling capacitor



| | | | |
|--|---------------------------|-------------------------------|----------|
|  同方国际信息技术有限公司 2F, No.240, Nienhu Rd, Nai-Hu Dist, Taipei, Taiwan, R.O.C. TEL:886-2-77188888 FAX:886-2-77218888 | | Unwill Technology Inc. | |
| File 60.BIOS.XTAL ,External SS ,M | | | |
| Size D Document Number GESK061 | | Rev V1. | |
| Date | Friday, December 23, 2016 | Sheet | 60 of 65 |

| STRAP2 | STRAP1 | STRAP0 | RAMCFG[4:0] | | | |
|--------|--------|----------|------------------|--------------------|----------|------------|
| L | L | L | 00000 | | | |
| L | L | H | 00001 | | | |
| L | H | L | 00010 | | | |
| L | H | H | 00011 | | | |
| H | L | L | 00100 | | | |
| ROM_SO | ROM_SI | ROM_SCLK | SOR_EXPOSED[3:0] | 1:ENABLE 0:DISABLE | | |
| L | L | L | 1111 DEFAULT | SOR0/1/2/3 ENABLE | | |
| L | L | H | 1110 | | | |
| L | H | L | 1101 | | | |
| L | H | H | 1100 | | | |
| H | L | L | 1011 | | | |
| H | L | H | 1010 | | | |
| H | H | L | 1001 | | | |
| H | H | H | 1000 | | | |
| L | L | M | 0111 | | | |
| L | M | L | 0110 | | | |
| L | M | H | 0101 | | | |
| L | H | M | 0100 | | | |
| H | L | M | 0011 | | | |
| H | M | L | 0010 | | | |
| H | M | H | 0001 | | | |
| H | H | M | 0000 | | | |
| STRAP5 | STRAP4 | STRAP3 | SMB_ALT_ADDR | DEVID_SEL | PCIE_CFG | VGA_DEVICE |
| M | H | H | 1 | 1 | 1 | 1 |
| M | H | L | 1 | 1 | 1 | 0 |
| M | L | H | 1 | 1 | 0 | 1 |
| M | L | L | 1 | 1 | 0 | 0 |
| L | H | M | 1 | 0 | 1 | 1 |
| L | M | H | 1 | 0 | 1 | 0 |
| L | M | L | 1 | 0 | 0 | 1 |
| L | L | M | 1 | 0 | 0 | 0 |
| H | H | H | 0 | 1 | 1 | 1 |
| H | H | L | 0 | 1 | 1 | 0 |
| H | L | H | 0 | 1 | 0 | 1 |
| H | L | L | 0 | 1 | 0 | 0 |
| L | H | H | 0 | 0 | 1 | 1 |
| L | H | L | 0 | 0 | 1 | 0 |
| L | L | H | 0 | 0 | 0 | 1 DEFAULT |
| L | L | L | 0 | 0 | 0 | 0 |

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

N17E-G1 VRAM Strap pin define

| Memory Density | Allowed Memory Configuration | FBUS/IO | Vendor | Manufacturer Part Number | Die Revision | Memory Speed | Memory Speed Grade | Data Code Alert | Test Plan | Status |
|----------------|------------------------------|---------|--------|--------------------------|--------------|--------------|--------------------|-----------------|-----------|------------|
| 8 GB | 256MB/512 | 1.8V | Apacer | AS5C1601-0408-B0A | B-00A | 8000 | 8000 | Full | Full | Production |

R2802 for MICRON VRAM
R2811 for SAMSUNG VRAM

60 STRAP0
60 STRAP1
60 STRAP2

N17E-Q1 VRAM Strap pin define

| Memory Density | Allowed Memory Configuration | FBUS/IO | Vendor | Manufacturer Part Number | Die Revision | Memory Speed | Memory Speed Grade | Data Code Alert | Test Plan | Status |
|----------------|------------------------------|---------|--------|--------------------------|--------------|--------------|--------------------|-----------------|-----------|------------|
| 8 GB | 256MB/512 | 1.8V | Apacer | AS5C1601-0408-B0A | B-00A | 8000 | 8000 | Full | Full | Production |

60 STRAP3
60 STRAP4
60 STRAP5

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL

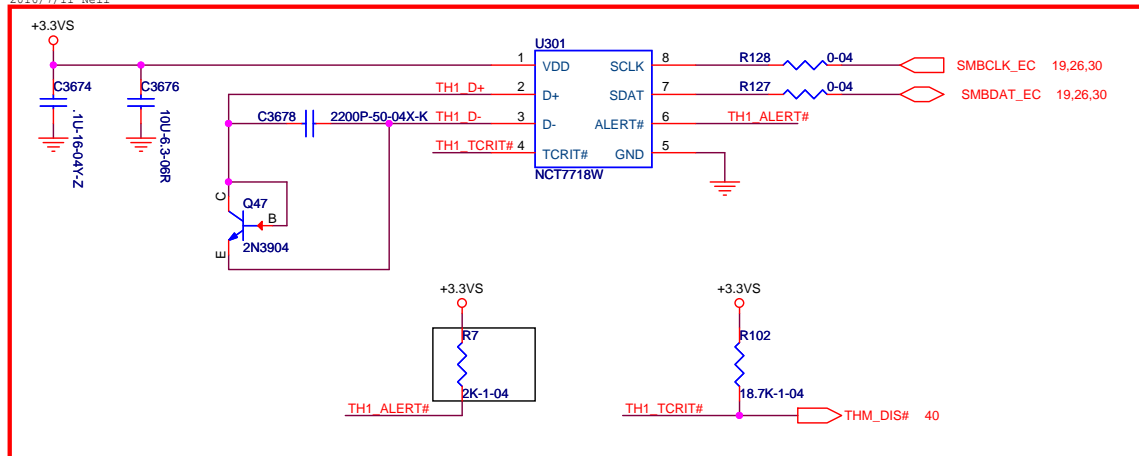
1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

60 ROM_SI
60 ROM_SO
60 ROM_SCLK

Thermal

2016/7/11 Neil



ALERT# /T CRIT# Pull-up Resistor

T_CRIT temperature strapping point

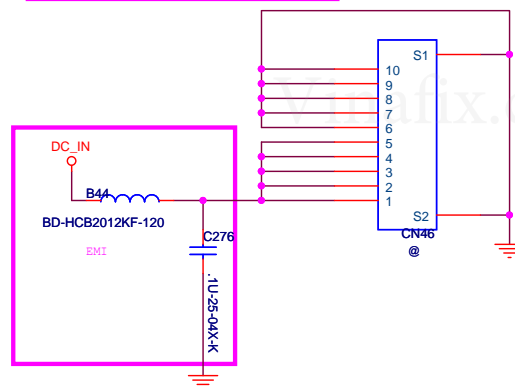
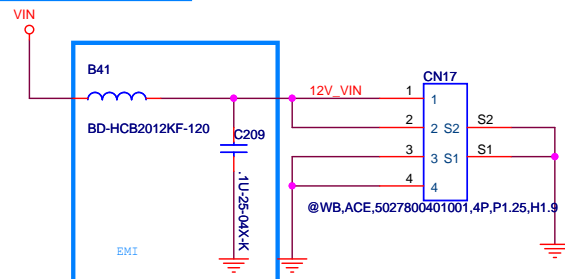
| R7 | R102 | 2KΩ | 7.5KΩ | 10.5KΩ | 14KΩ | 18.7KΩ |
|--------|------|------|-------|--------|-------|--------|
| 2KΩ | 77°C | 87°C | 97°C | 107°C | 117°C | |
| 7.5KΩ | 79°C | 89°C | 99°C | 109°C | 119°C | |
| 10.5KΩ | 81°C | 91°C | 101°C | 111°C | 121°C | |
| 14KΩ | 83°C | 93°C | 103°C | 113°C | 123°C | |
| 18.7KΩ | 85°C | 95°C | 105°C | 115°C | 125°C | |

Layout notice:

- *Put the C3678 2200pF to close the NCT7718W.
- *Add ground shielding for D+ and D- traces.
- *D+/D- route has to be away from the high noise area.
- *The recommended traces width and ground shielding spacing are 10mils.


For HTC 12V

For VR Charger DB



VA:
1.HDMI pull high電阻(GE5SN71 DCN): P.29
2.BAT 18A: P.36
3.VCCGT(GE5SN71 DCN): P.42
4.FBVDDQ(GE5SN71 DCN): P.58
5.EDP form GPU(G-SYNC預留): P.28, P.30, P.59, P.61
6.4 area RGB BL: P.30, P.44
7.HDD NVMe: P.32
8.4.1 sound system: P.34
9.GPU Strap 0 default set Samsung VRAM: P.62
10.Thermal IC function: P.40, P.63
11.HTC 12V VIN from MB: P.63
12.Type C sequence(GE5SN71 DCN): P.40, P.45
13.Power JP點: P.38, P.39, P.41-P.43, P.53
14.USB3.1 PCIE 13換PCIE 6: P.17, P.18, P.45
15.LID#預留pull high: P.30
16.+1.25VS VIN JP改0-04: P.41
17.Add two AMP for 4 speaker output: P.34, P.18
18.Optimus PEX_RST#預留: P.46
19.MAX-Q GPIO3 pull high預留: P.61
20.PCB hole disconnect to GND: P.37
21.EMI預留: P.63, P.44
22.intel EDP disable: P.8, P.20
23.CN43,CN44(85W FAN CONN) delete: P.35
24.VCCIO choke size smaller, C3747&C3745 change 0603: P.39
25.4 area RGB KB BL 10 pin connector: P.44, P.19, P.18

VB:
(1)CN15, CN33 change footprint&value(SMT bug): P.35
(2)R3306 change 0805, 10 ohm and parallel R3325(10-08)(Mike suggest): P.36
(3)4 area KB RGB BL HW board ID(Bios request): P.24, P.44
(4)R3546 change 1K(driving higher for LCD PWM): P.28
(5)R165 OP, pull high 3.3V_LCD 100K(R951) on PANEL_3.3V_ON let EC to turn on/off LVDS_VIN: P.18,P.28
(6)R3324(100 ohm) series BAT temp net(ITE suggest): P.36
(7)R3544 change 10K(driving higher for BL_ON): P.28
(8)R912 change 100 ohm(LCD sequence): P.28
(9)R873 stuff(DGPU power off sequence): P.53
(10)U13 & U18's pin 5 & pin 6(Rin & Lin) connect LINE2 signal: P.34
(11)L62 change footprint(SMT bug): P.39
(12)Add VR charger DB connector CN46: P.63
(13)PS5 change footprint(SMT bug): P.37
(14)4 area KB RGB BL pin 7 & pin 8 change to connect PCH_SMB_DATA & PCH_SMB_CLK(bios request): P.44, P.19
(15)預留R189 for GPIO13 LCD_BLEN_EC connect to PCH_BL_EN(EC Request): P.30
(16)R2902 change 2.7K, R2868 change 2K(Oscar suggest): P.54
(17)ACN1 connect to U7 SPK out: P.34
(18)LID function(stuff:R982,R909,C1338,R910,R189 OP:R983,R130,R154) (EC&BIOS request): P.28, P.30
(19)D37,D52,D53 change SGZ005C80 (EMI request): P.44
(20)Add C1375(1uf) (EMI request): P.34
(21)當機+VCCCORE disappear:
A.+VCCCORE capacitor 0805 change 47Uf: P.42,
C575,C585,C582,C577,C574,C3334,C3337,C619,C654,C657,C658,C3336,C3333,C584,C3346,C3345,C3344,C3343,C583
B.+VCCCORE add capacitor C376 470Uf, C388&C377 change 470uf
C.C600,C640,C642 change .22Uf
D.R758 change 10 ohm
(22)R3197 change 47K FOR 天冷開機黑屏: P.41
(23)Change 1U-6.3-04R-K FOR PUR: C126,C131,C139,C142,C162,C175,C177,C196,C669,C290,C291,C353,C355,C491 : P.30,P.34,P.28,P.44,P.36

| | | | |
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| Title 64.Change list | | | |
| Size B | Document Number GE5KN61 | | Rev V1.0 |
| Date: | Friday, December 23, 2016 | Sheet 64 | of 65 |

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| File | | | |
| 65.History | | | |
| Size | Document Number | | Rev |
| C | GE5KN61 | | V1.0 |
| Date: | Friday, December 23, 2016 | Sheet | 65 of 65 |